

KRM-5ZUxxEG

KEY FEATURES

- Xilinx MPSoC
- 120 HD I/O (5 Banks)
- 52 HP I/O (1 Bank)
- 52 PS MIO (501 & 502)
- 24+4 GTH/GTP Transceivers
- up to 8GB 64 bit DDR4 PS RAM
- up to 8GB 64 bit DDR4 PL RAM
- eMMC and QSPI
- 12V supply



The KRM-5ZUxxEG Module provides the optimal balance of I/O capabilities, Memory bandwidth and transceiver count.

Maximum memory bandwidth

The 64 bit wide DDR4 PL interface operates at 2.4GT/s and provides valuable memory bandwidth to PL logic without taxing the PS AXI interfaces or reducing the APU's access to PS DDR4. This leads to substantially enhanced performance for a multitude of designs where PS/PL co-processing and buffer needs are essential. Prime examples are image processing with deep temporal filters or acceleration of ML inference for edge devices.

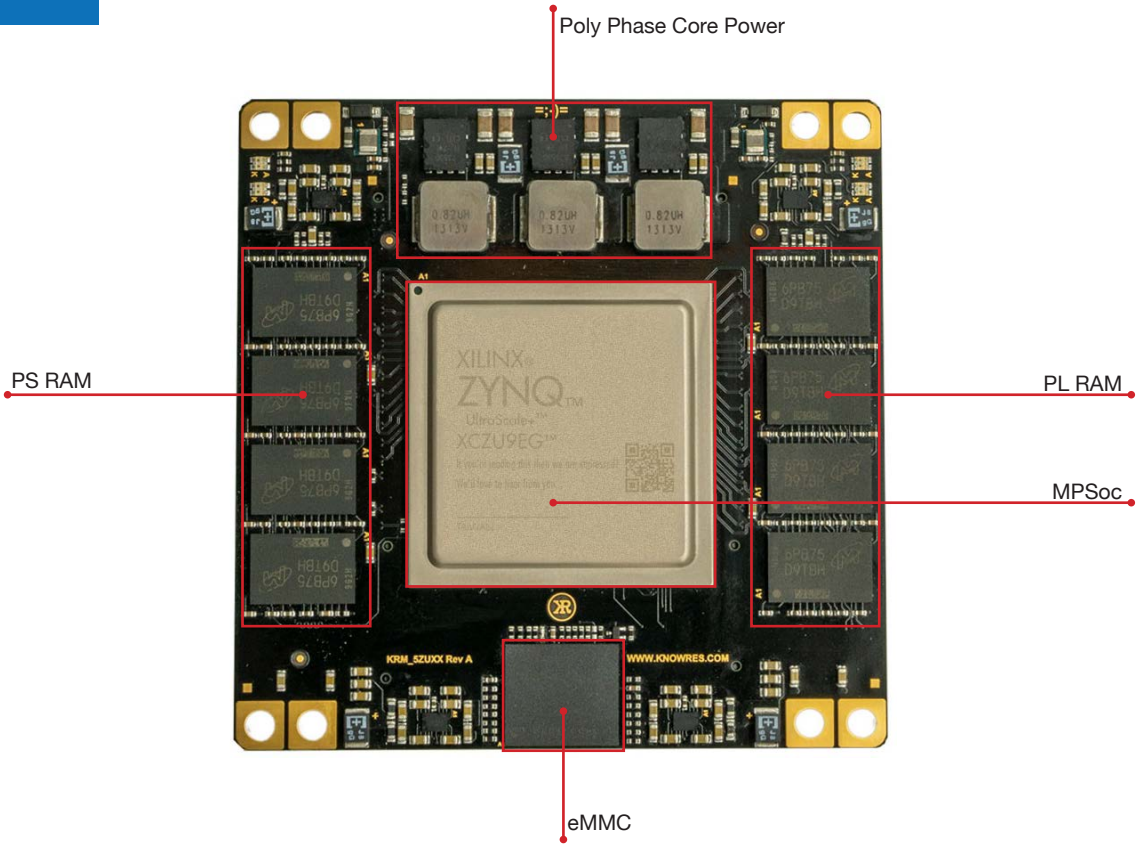
Designed to scale

The KRM-5ZUxx Module family is designed as a common form factor for MPSoC's ranging all the way to ZU19EG. The regulator stages are dimensioned for a maximum module power in excess of 100W which provides more power headroom than any other module with a comparable form factor currently (Q2 2020) on the market.

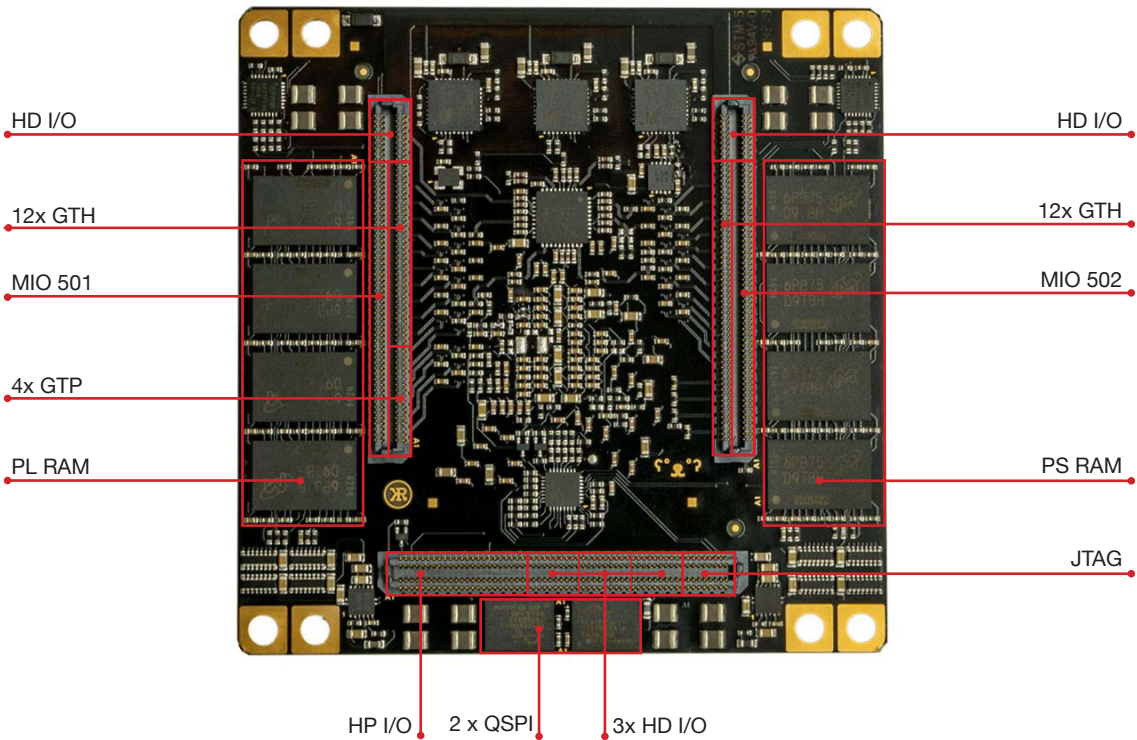
Easy integration

The KRM-5ZUxxEG Module only requires a 12V power supply and the application specific peripherals to create a complete system. Power management, sequencing, reset and boot memory are all on-board and ready to run. KR will provide reference designs for carriers, PL Logic and APU code.

TOP



BOTTOM



FEATURES

CORE COMPONENT

- Xilinx XCZU9EG-1FFVB1156-E standard
- Any MPSoC in the FFVB1156 package as an option

PROCESSING SYSTEM

- Quad Core ARM Cortex™- A53
- Dual Core ARM Cortex™-R5

FPGA FABRIC

- Xilinx Ultrascale+™ fabric
- 215k- 341k 6-input LUT
- 429k- 682k flip flops
- 25.1-32.1Mb BRAM
- 0 – 22.5Mb UltraRAM
- 1973-3528 DSP slices

MEMORY OPTIONS

- 64 bit DDR4 PS RAM 2-8GB @ 2.4GTs
- 64 bit DDR4 PL RAM 2-8GB @ 2.4GTs
- eMMC to 64GB
- QSPI to 1GB

MODULE I/O

- 120 HD I/O (5 banks 1V8 to 3V3)
- 52 HP I/O (1 bank 1V5 to 1V8)
- 52 PS MIO (2 banks 1V8 to 3V3)
- 24 GTH transceivers to 16Gb/s
- 8 external reference inputs
- 4 PS GTP transceivers to 6.6 Gb/s
- 4 external reference inputs
- BMC UART / PS UART
- BMC Status signals (CFG Done, POK etc)
- JTAG
- RESET in

POWER

- 12V input (11.5V-12.5V)
 - Low noise, poly phase vcc-int converter
 - Fully digital supply with telemetry
- Separate & configurable supply outputs for each MIO and PL IO bank (4 total)
 - 1A supply max each

CLOCKING

- 3: 8 clock tree
 - All digital module elements can be derived from one on-board master clock
 - External clock or on-board master oscillator
 - Two external differential clock inputs
- On-Board Clock-synthesis for
 - PL DDR4 interface reference clocks (2x)
 - 4 PL GTH reference clocks (two per side)
 - PS clock
- Off-board clock inputs
 - GTH references (four per side)
 - GTP reference clocks (one per transceiver)

BMC

- Board Management Controller for
 - Clock configuration
 - Power sequencing & telemetry
 - Boot mode selection
 - Status signalling

DIMENSIONS

- 75x75 mm
- 15mm max. height with heat-spreader

ENVIRONMENTAL

- Extended temperature or industrial temperature range

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