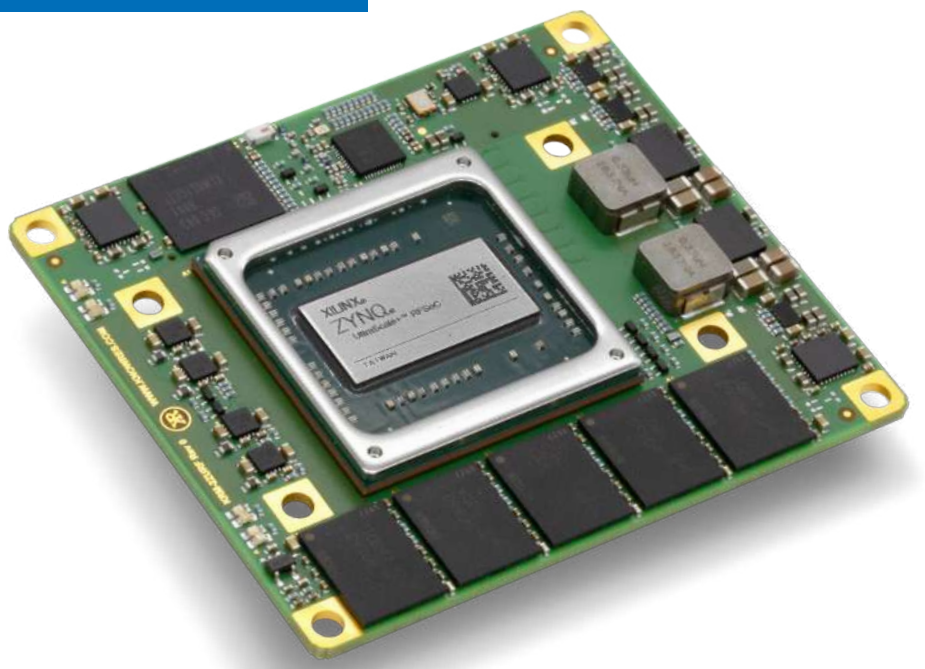
PRODUCT SHEET
KRM-2ZUxxDR

KRM-2ZUxxDR

KEY FEATURES

- AMD RFSoC DFE
- 8 x ADC @ 2.95 GSPS
- 2 x ADC @ 5.9 GSPS
- 8 x DAC @ 10.0 GSPS
- 24 HD IO
- 52 PS MIO
- 8+4 GTY/GTR Transceivers
- 72 bit ECC PS DDR4 RAM
- 48 bit PL DDR4 RAM
- 75x65mm small



The KRM-2ZUxxDR module features the most versatile design so that it can be optimally utilized in a multitude of applications.

Most Capable RFSoC

AMD's RFSoC DFE family features an enhanced analog bandwidth of 7.125GHz, up from 6GHz on Gen3 and 4GHz on Gen1 devices. The additional bandwidth makes higher Nyquist zone applications feasible.
The DFE hard IP and Low Phy hard IP blocks such as Channel filter, DUC/DDC, MIXER, and FFT/iFFT implement common functions in an energy efficient way. The balanced blend of hard IP and sizeable FPGA fabric with almost 500k System Logic cells and more than 1800 DSP Blocks makes this family exceptionally capable in a broad range of wireless applications.

Wrapped in our reliable system design and implemented in a compact 75x65mm form factor, the KRM-2 SoM is the perfect choice to deploy this marvel of a chip.

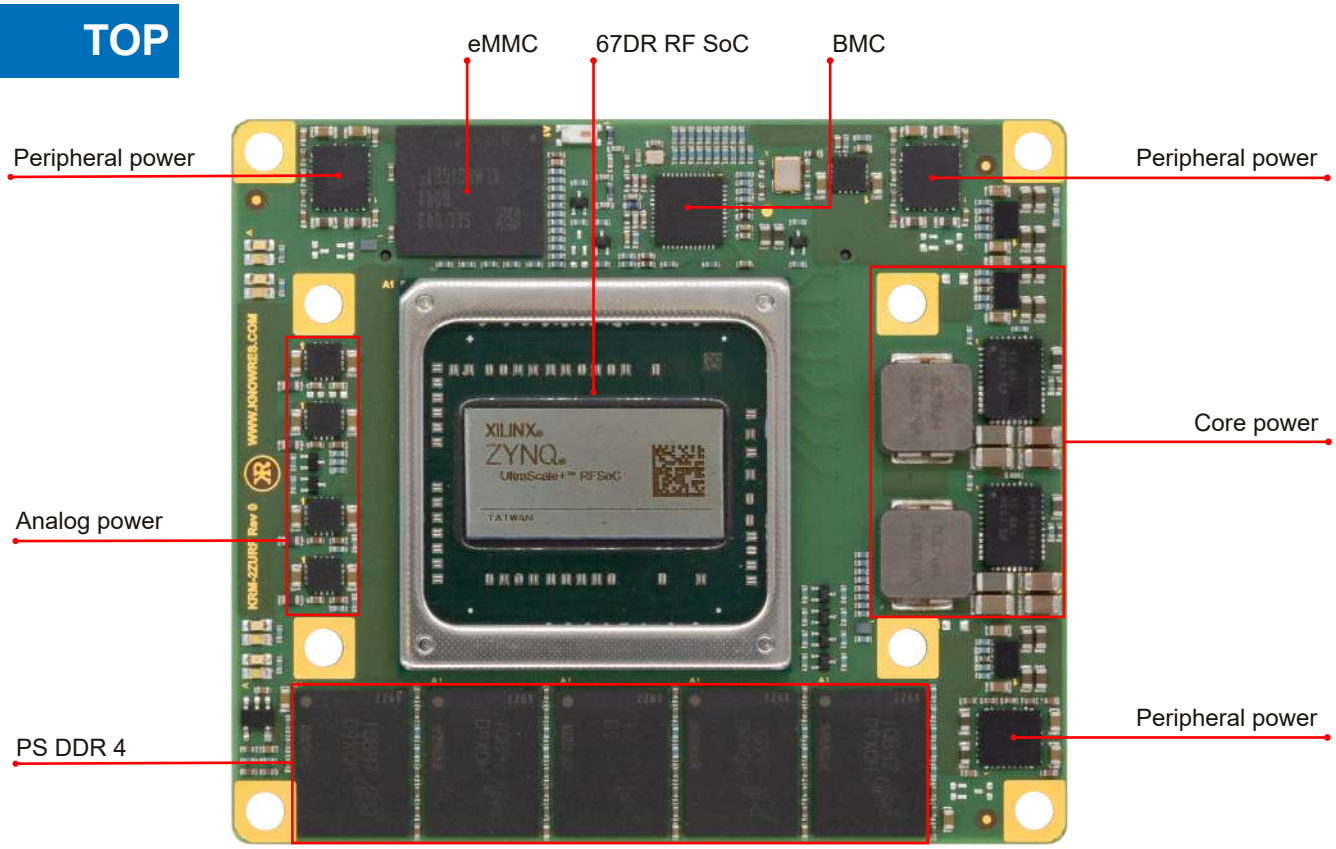
Flexible RF Section

The RF ADC and DAC interfaces are designed for maximum flexibility. The module generates its own ultra-low noise analog supply voltages. The LDO supplied voltages are available on X1 and can be used by the analog front end carrier board. Alternatively, if the analog front end requires more power than available from the module, the RF baseboard may provide the RFSoC ADC/DAC with low noise power or operate on independent power rails. RF Sample clocks are to be implemented on the RF carrier, so that the system designer can implement the optimal clocking for the desired application.

Easy Integration

The KRM-2ZUxxDR module only requires a 12V power supply and the application specific peripherals to create a complete system. Power management, sequencing, reset and boot memory are all on-board and ready to run. KR provides reference designs for carriers, PL Logic and APU code to any qualified party to accelerate the design-in process.

TOP



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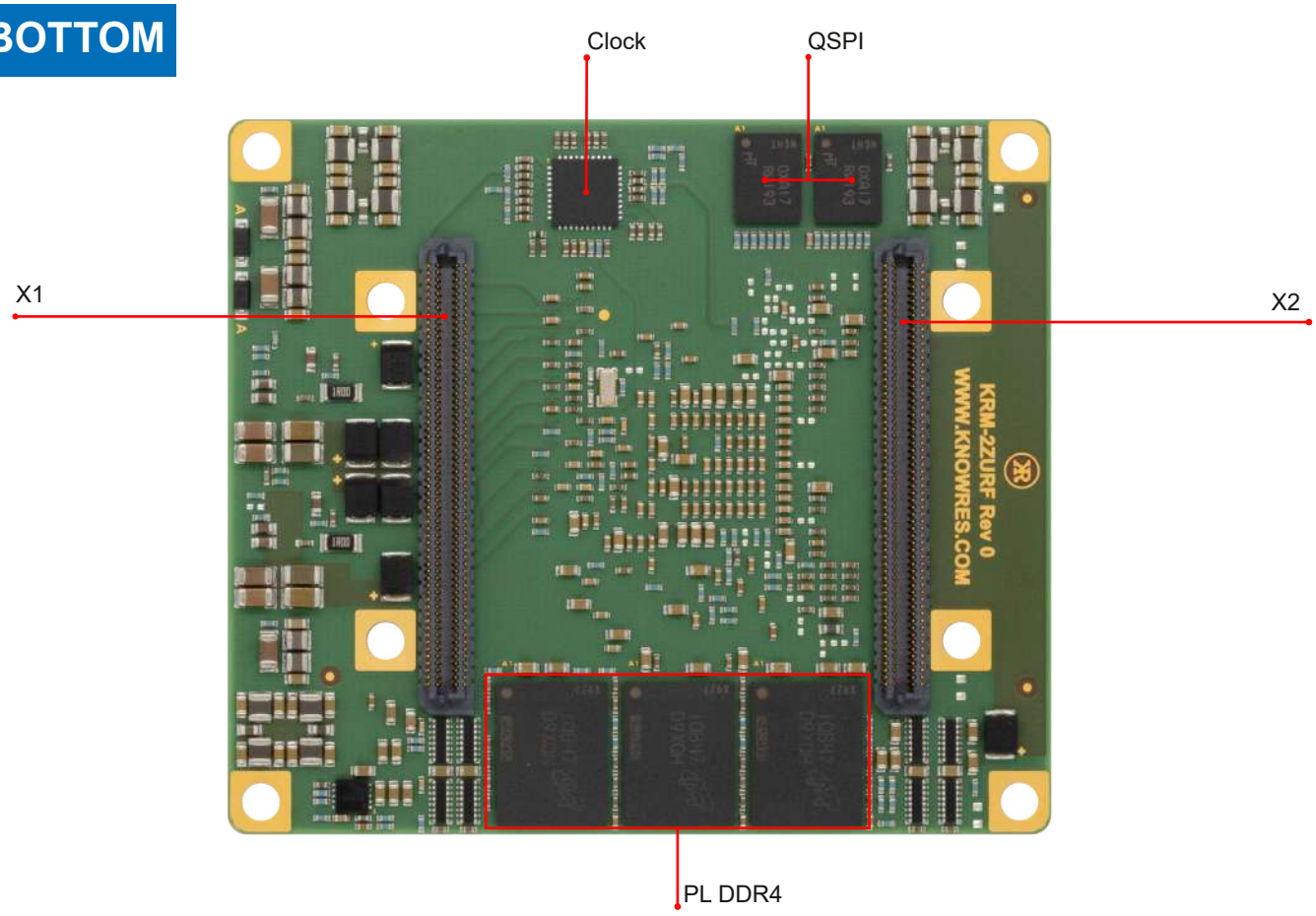

FEATURES

Core Component Options
- Xilinx XCZU67DR-2FSVE1156-E

Processing System
- Quad Core ARM Cortex™- A53
- DUAL Core ARM Cortex™-R5

FPGA Fabric
- Xilinx Ultrascale+™ fabric
- 244k 6-input LUT
- 488k flip flops
- 6.8Mb BRAM
- 45 MB UltraRAM
- 1872 DSP slices

Memory Options
- 72 bit DDR4 PS ECC RAM 8GB @ 2.4GTs
- 48 bit DDR4 PL RAM 6GB @ 2.4GTs
- eMMC up to 64 GB
- 1 Gb QSPI

Module I/O
- 8x RF ADC 2.95 GSPS
- 2x RF ADC 5.9 GSPS
- 8x RF DAC 6.554/10.000 GSPS
- 24 HD I/O (1 bank 1V8 to 3V3)
- 52 PS MIO (2 banks 1V8 to 3V3)
- 8 GTY transceivers to 32Gb/s
  - 4 external reference inputs
- 4 PS GTP transceivers to 6.6 Gb/s
  - 4 external reference inputs
- BMC UART / PS UART
- BMC Status signals (CFG Done, POK etc)
- JTAG
- RESET

Power
- 12V input (11.5V-12.5V)
  - Low noise, poly phase vcc-int converter
  - Fully digital supply with telemetry
- Separate & configurable supply outputs for each MIO and PL IO bank
  - 1A supply max each

Clocking
- 3:4 clock tree
  - All digital module elements can be derived from one, on-board master clock
  - External clock or on-board master oscillator
  - Two external differential clock inputs
- On-board clock synthesis
  - PL DDR4 interface reference clock
  - 2 PL GTY reference clocks (one per quad)
  - PS clock
- Off-board clock inputs
  - GTY references (one per quad)
  - GTP reference clocks (one per transceiver)
  - RF ADC
  - RF DAC
  - Sysclock and Sysref for MTS support

BMC
- Board Management Controller for
  - Clock configuration
  - Power sequencing & telemetry
  - Boot mode selection
  - Status signaling

Dimensions
- 75x60 mm
- 15 mm max. height with heat-spreader

Environmental
- Extended temperature or industrial temperature range