KRM-4ZUxxDR

KEY FEATURES

- Xilinx RFSoC Gen1/3
- 8x RF ADC and DAC
- 48 HD I/O
- 52 PS MIO
- 16+4 GTY/GTR transceivers
- Up to 8 GB 64-bit DDR4 PS RAM
- 2 instances of up to 8 GB 64-bit DDR4 PL RAM
- eMMC & QSPI

The KRM-4ZUxxDR module features the most versatile design so that the module can be optimally utilized in a multitude of applications.

Best Memory Bandwidth

The dual 64-bit wide DDR4 PL interfaces, operating at 2.4GT/s, provide the highest PL memory bandwidth of any currently available RFSoC module (2024). This memory bandwidth is in addition to the 64-bit wide PS DDR4 interface and can be used as fast and deep sample acquisition memory, waveform memory for high speed pattern generation or deep FIFOs for complex multi-stage DSP operations. Due to the independent interfaces, truly concurrent read and write operations are natively supported.

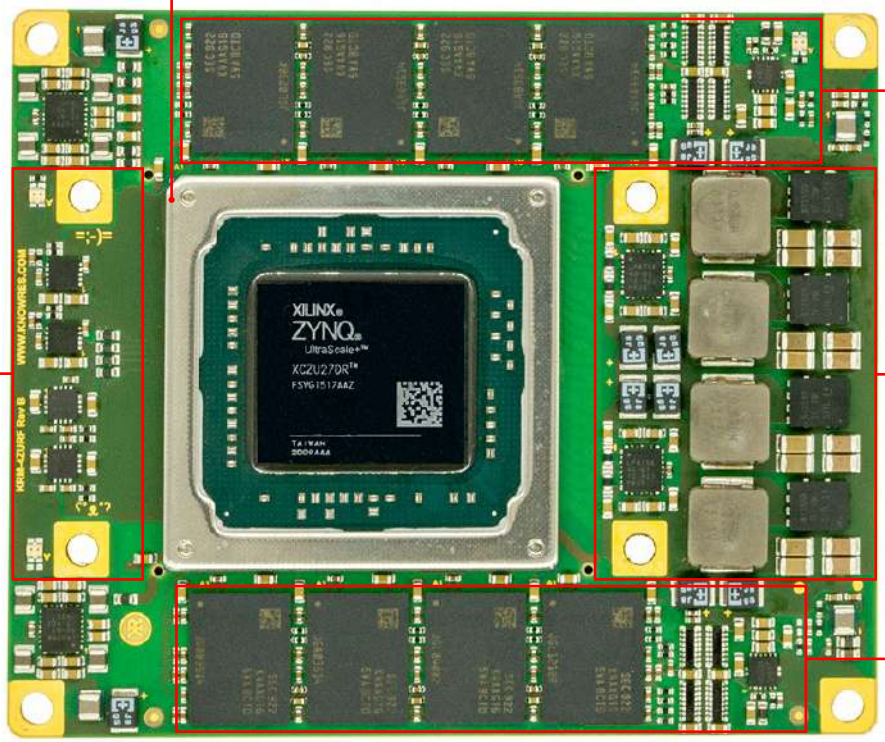
Flexible RF Section

The RF ADC and DAC interfaces are designed for maximum flexibility. The module generates its own ultra-low noise analog supply voltages. The LDO supplied voltages are available on X1 and can be used by the analog front end carrier board. Alternatively, if the analog front end requires more power than available from the module, the RF baseboard may provide the RFSoC ADC/DAC with low noise power or operate on independent power rails. RF Sample clocks are to be implemented on the RF carrier, so that the system designer can implement the optimal clocking for the desired application.

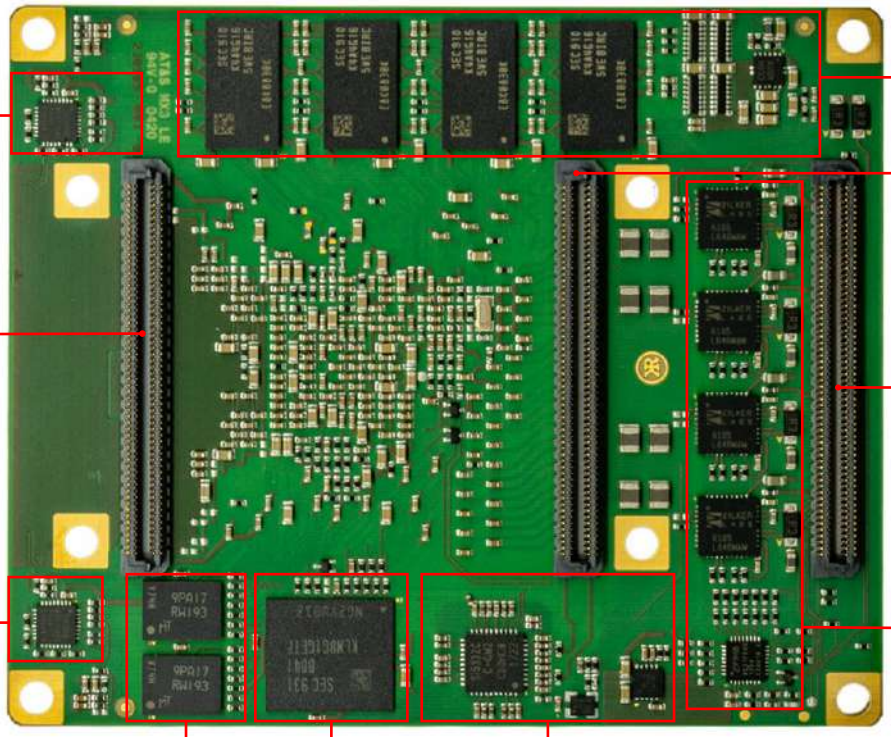
Easy Integration

The KRM-4ZUxxDR module only requires a 12V power supply and the application specific peripherals to create a complete system. Power management, sequencing, reset and boot memory are all on-board and ready to run. KR provides reference designs for carriers, PL Logic and APU code to any qualified party to accelerate the design-in process.

TOP



BOTTOM



FEATURES

Core Component

- Xilinx XCZU27DR-1FFV1517-E standard
- Any RFSoC in the FFV/FSV1517 package as an option

Processing System

- Quad Core ARM Cortex™-A53
- DUAL Core ARM Cortex™-R5

FPGA Fabric

- Xilinx Ultrascale+™ fabric
- 310k- 425k 6-input LUT
- 620k- 850k flip flops
- 27.8-38 Mb BRAM
- 13.5 – 22.5 Mb UltraRAM
- 3145-4272 DSP slices

Memory Options

- 64-bit DDR4 PS RAM 2-8GB @ 2.4GTs
- 2 instances of 64-bit DDR4 PL RAM 2-8 GB @ 2.4GTs
- eMMC up to 64 GB
- 1 Gb QSPI

Module I/O

- 8x RF ADC 4.096/5.0 GSPS (GEN1/3)
- 8x RF DAC 6.554/10.0 GSPS (GEN1/3)
- 48 HD I/O (2 banks 1V8 to 3V3)
- 52 PS MIO (2 banks 1V8 to 3V3)
- 16 GTY transceivers to 32Gb/s
  - 4 external reference inputs
- 4 PS GTP transceivers to 6.6 GB/s
  - 4 external reference inputs
- BMC UART / PS UART
- BMC Status signals (CFG Done, POK etc)
- JTAG
- RESET in

Power

- 12V input (11.5V-12.5V)
  - Low noise, polyphase vcc-int converter
  - Fully digital supply with telemetry
- Separate & configurable supply outputs for each MIO and PL IO bank (4 total)
  - 1A supply max each

Clocking

- 3:8 clock tree
  - All digital module elements can be derived from one on-board master clock
  - External clock or on-board master oscillator
  - Two external differential clock inputs
- On-board clock-synthesis for
  - PL DDR4 interface reference clocks (2x)
  - 4 PL GTY reference clocks (one per quad)
  - PS clock
- Off-board clock inputs
  - GTY references (one per quad)
  - GTP reference clocks (one per transceiver)
  - RF ADC
  - RF DAC

BMC

- Board Management Controller for
  - Clock configuration
  - Power sequencing & telemetry
  - Boot mode selection
  - Status signalling

Dimensions

- 90 x 75 mm
- 15 mm max. height with heat-spreader

Environmental

- Extended temperature or industrial temperature range