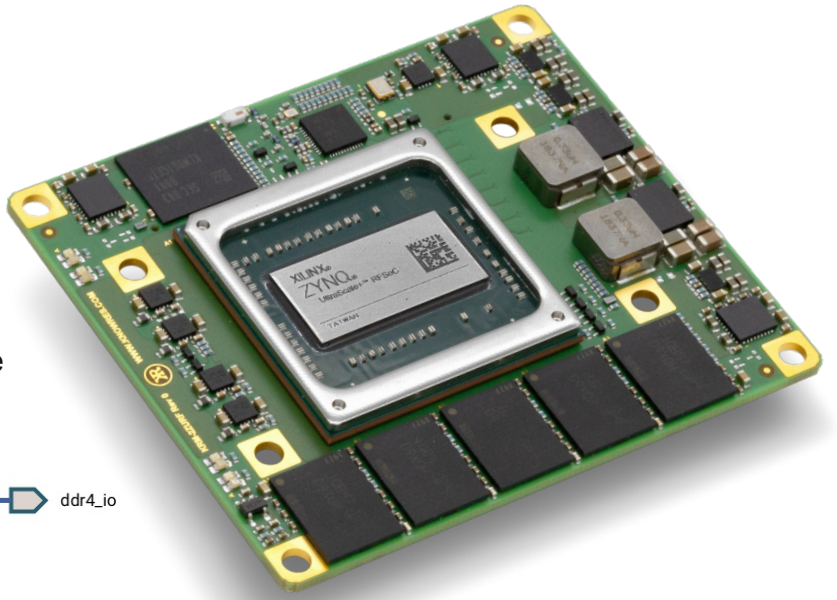
PRODUCT SHEET
KR-DDR4 Memory Controller IP

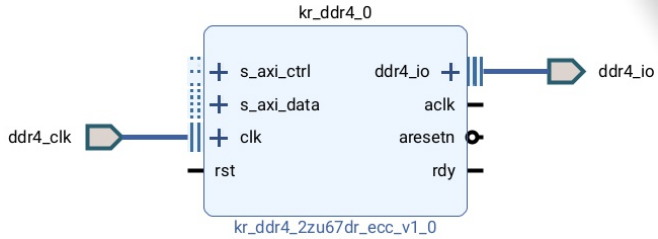
KR-DDR4 IP

KEY FEATURES

Fit more logic.

KR-DDR4 IP is a compact, high-performance memory controller tailored for use with PL DDR4 memory on AMD/ Xilinx UltraScale+ families of Knowledge Resources SoMs.

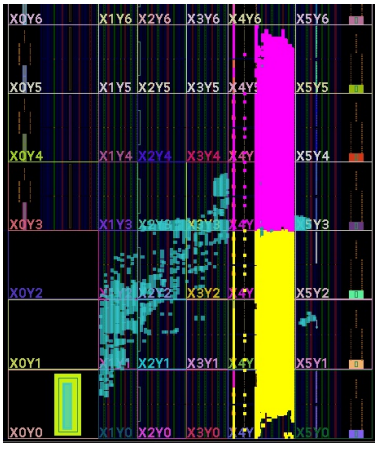




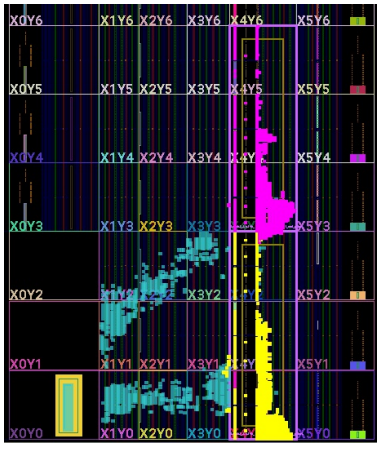
FEATURES & BENEFITS

- Full DDR4 memory controller including PHY layer
- Pre-calibrated SoM-specific PHY configuration tested for thermal stability
- Very small footprint:
  - more than 4x lower CLB usage compared to AMD/ Xilinx MIG DDR4 v2.2[1]
  - zero BRAM/DSP usage
- High performance:
  - 2400 MT/s
  - 89% / 89.8% / 78 % efficiency for sequential Write/ Read/Read-Write
  - sub-millisecond (< 500 us) core initialization time
- 128- / 256- / 512-bit wide AXI4 data interface[2]
- 128- / 256- / 384- / 576-bit wide native data interface[3]
- ECC support with AXI4-Lite control/status interface4
- Easy to use:
  - available as Vivado IP packages (Verilog HDL and pre-synthesized EDF)
  - integrated synthesis/implementation constraints
  - Vitis Classic/Unified software driver support

[1]FPGA resource usage for a dual 512-bit DDR4 controller design on KRM-4ZU47DR SoM
[2,3,4]depending on the SoM



AMD/Xilinx MIG DDR4 v2.2



KR-DDR4