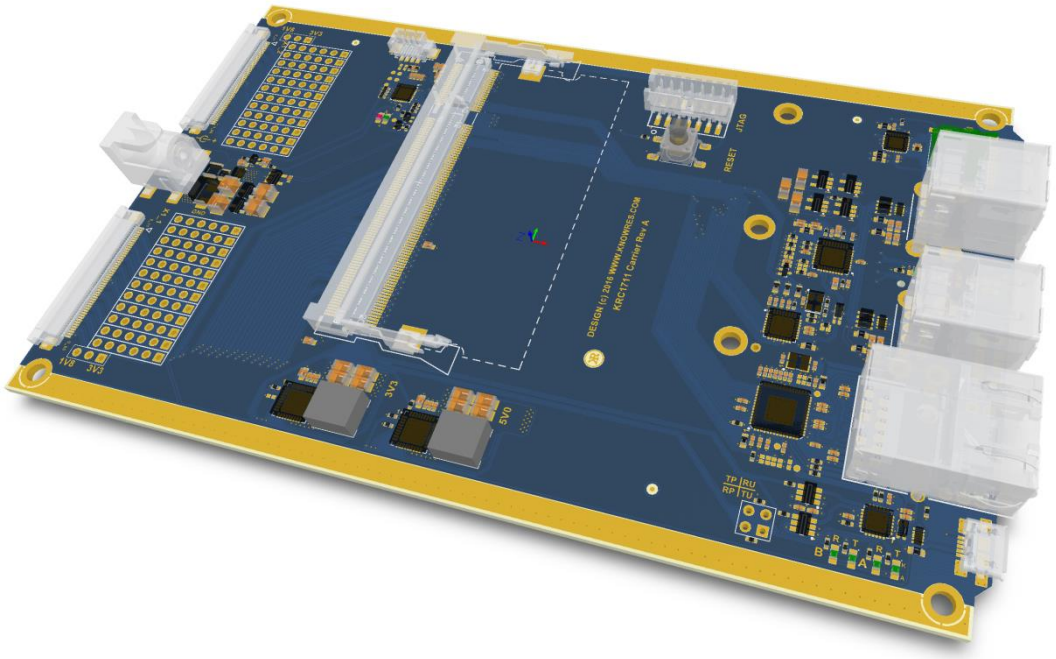
KNOWLEDGE RESOURCES
Switzerland GmbH

KRC1711-CARRIER

Data sheet



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Revision History

Date	Document revision	HW revision	Changes
Sept 27th 2016	0.1	REV A	Import KRC1710
Sept 29th 2016	1.0	REV A	First public release, changed to KRC1711 Removed old errata Updated Images
October 22th 2019	1.1	REV A	Added Company telephone number and e-mail Updated Company address Removed Advance Mode paragraph Updated standard disclaimer Added Maximum ratings Added recommended operating conditions Added compliance statement

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Assumptions

The reader is familiar with Xilinx FPGA and SoC components and the related terminology in common use.

Acronyms

FU:	Future Use
KR:	Knowledge Resources GmbH
MGT:	Multi Gigabit Transceiver
NA:	Not Applicable
PL:	Programmable Logic
PS:	Processing Subsystem
SoC:	System on Chip
SoM:	System on Module
uC:	Microcontroller

Reference documents

ZYNQ all programmable SoC, Xilinx, www.xilinx.com

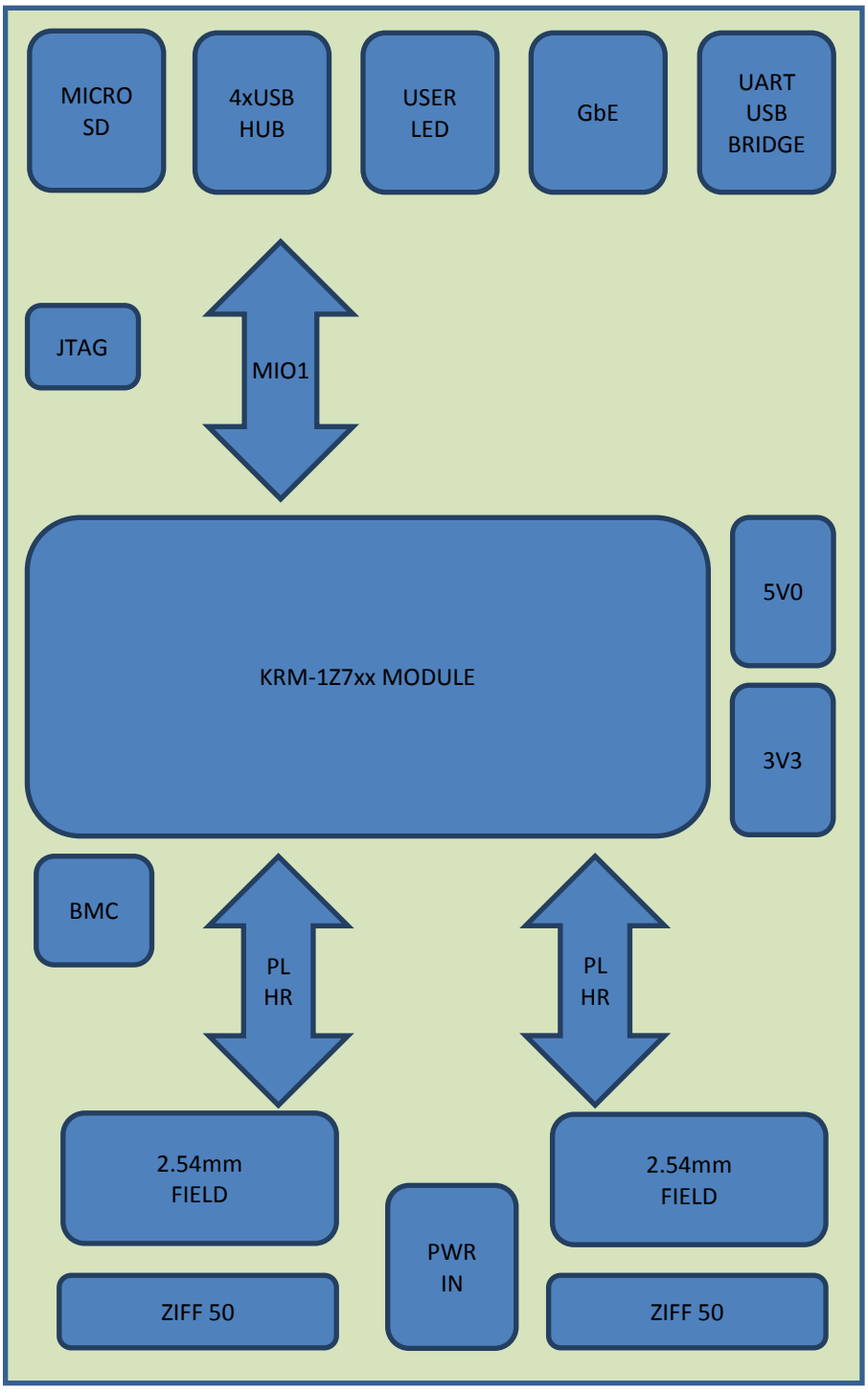
Support

Support to aid in customer specific design-in is available at competitive rates, please contact KR for details:
+ 41 61 545 2080 or mail to office@knowres.com

Introduction

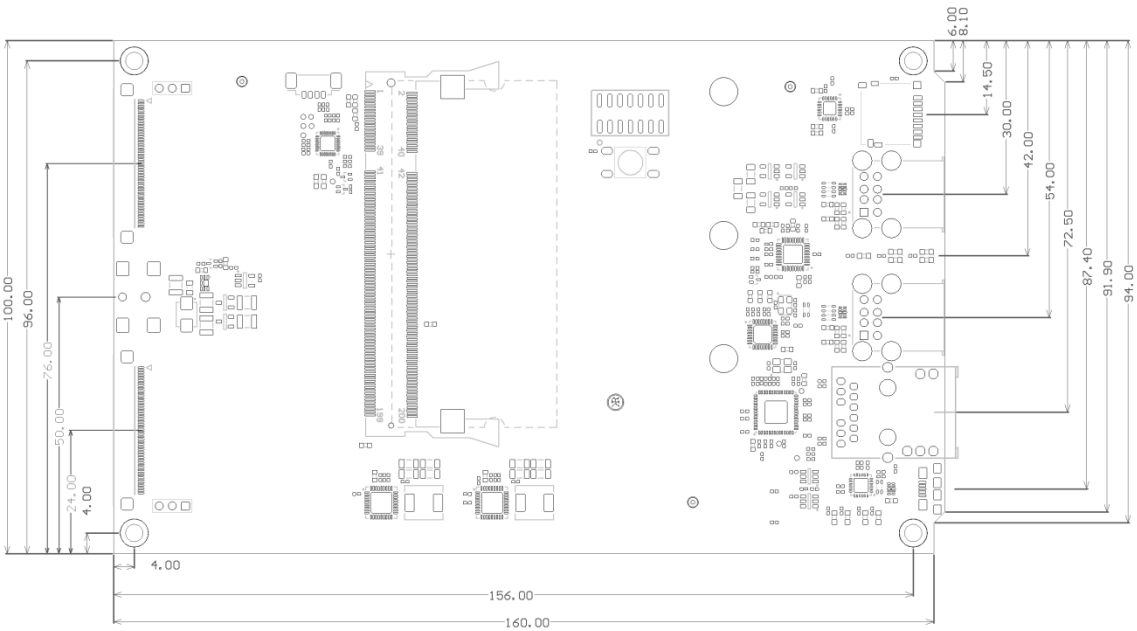
With the KRC1711, Knowledge Resources provides a highly flexible and cost-efficient evaluation board for embedded systems prototyping with KRM-1Z7xxx family modules. The carrier board offers all of the essential infrastructure elements that are required to operate a KRM-1Z7xxx family module. Furthermore, the PL ports are readily accessible via 50 pin Ziff expansion connectors, and a 2.54mm raster solder field.

The carrier has a Euro-card form factor of 100x160mm and fits into a Lansing “micropack c-style” enclosure, thereby facilitating the fabrication of complete small run projects without significant investments into custom enclosures.



Board dimensions

(in mm)



- Altium PCB and Schematic templates are available

Features

Overview

- Accepts KRM-1Z7xxx series modules
- Dual UART to USB bridge
- 1 x Micro SD Slot
- 4 x USB port (via 4 port hub)
- 1 x Gb Ethernet Port
- 2 x 50Pin Ziff Headers (one per PL Bank)
- JTAG debug port
- Single 12V DC supply input 2.1mm by 5.5mm barrel jack
- Configurable power manager

Power supply

Normal operating conditions

The KRC1711 is designed to accept 12V DC. A 12V power supply able to source at least 2A is recommended in order to fully support the range of modules and daughter cards that can be paired with the KRC1711.

The KRC1711 generates two “global” Voltages: 5V and 3V3. Each is capable of sourcing up to 6A. The inputs of the regulators are globally fused. The power OK status is monitored by the BMC.

The 3V3 Supply powers the KRM-1Z7xxx Module and several I/O peripheral circuits (such as the SD card socket). This power rail may also be used to power the PL I/O banks via jumper next to the 50pin ziff connectors.

The 5V0 Supply is used to power the USB ports and is the source for power converters on Ziff connector expansion modules.

A 1V8 supply is generated on the KRM module and powers a multitude of peripherals such as the USB Phy, Ethernet Phy, and parts of the SD card interface chip. This power rail may also be used to power the PL I/O banks via jumper next to the 50pin ziff connectors.

The KRC1711s input is reverse polarity, over-voltage and under-voltage protected.
- Reverse polarity will trip a self-healing fuse.
- The power manager monitors the input voltage and prevents the 12V soft start form being enabled if the input voltage exceeds 13V DC. This ensures that the following regulator’s input voltage limit is not exceeded. The power manager also monitors the supply after power up and will initiate an emergency shut down if the input voltage rises above 13V. The input overvoltage protection will fail if exposed to input voltages above 20V.
- The power manager also monitors the input voltage for an under voltage condition. It prevents power up if the voltage is below 7V DC, and initiates power down if the input voltage falls below 6V DC.

	PARAMETER	MIN	NOMINAL	MAX
PWR OPERATING CONDITIONS	V-IN	6V DC	12V DC	13V DC
	UVLO turn on limit	7V DC		
	UVLO turn off limit			6V DC
	OV power up limit	13V DC		
	I MAX continuous		2A	

Factory settings

In its factory configuration, the KRC1711 is configured to power up once a valid 12V supply is detected. This may be changed to a mode that requires a power up command on the power manager's serial console.

	PARMETER	DEFAULT	OPTION	REMARK
FACTORY DEFAULTS	Auto power on	ON	OFF	Within valid V-in range
	Baud rate	115200	N/A	

Control console

When the KRC1711 UART to USB console port is connected to a host PC, two virtual COM ports will be activated. The COM port numbers depend on the host system. One of the ports is connected to PS UART0 of the KRM-1Z7xxx module, the other COM port is connected to the power manager of the carrier.

Configure a terminal program to 115200 Baud, 8N1. Then use the command "KRC1711:?" for a list of supported commands and current status of the carrier board.
Every command to the KRC1711 must be preceded by "KRC1711:"

Example output of a KRCxxx power manager:

Reset

The KRM-1Z7xxx modules generate their own on board power on reset. A user reset button for the PS of the Zynq on a KRM-1Z7xxx module is available.
The reset signal is also routed to the JTAG connector therefore enabling full debug support for the ARM cores.

JTAG

A 14 pin header that is compatible with the Xilinx USB Platform-cable or Digilent Programming adapters gives the developer JTAG access to the Zynq on the module.

JTAG Signals:

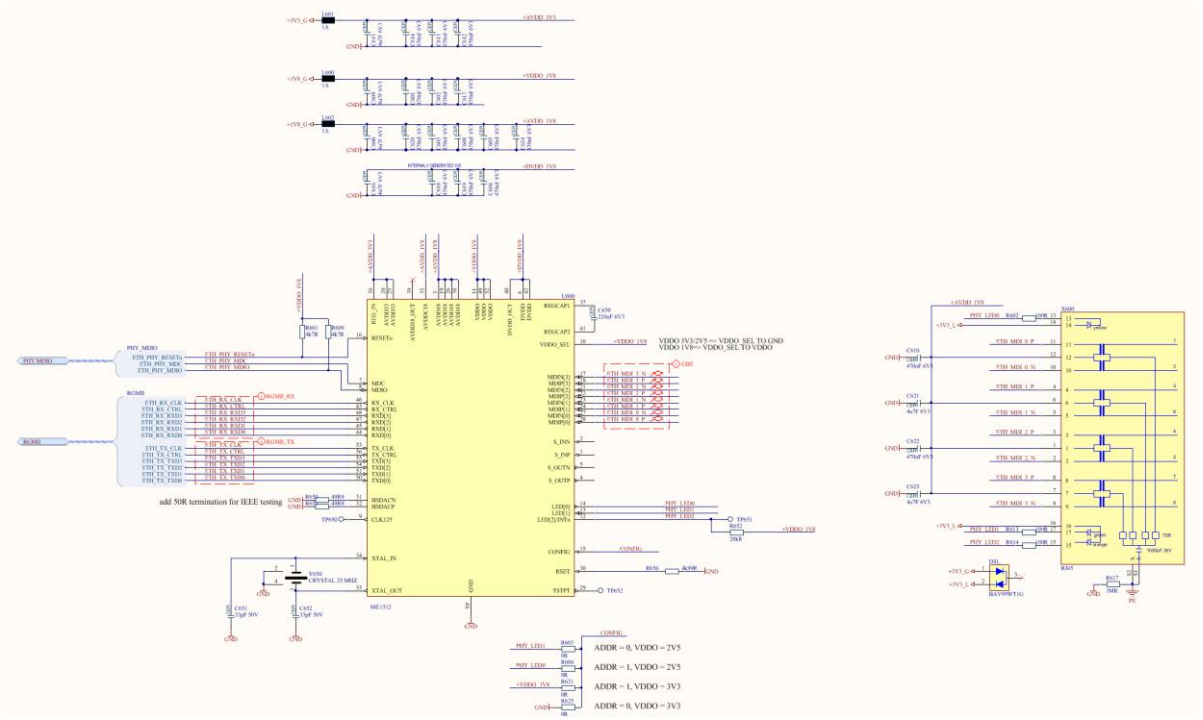
	PGM HEADER	KRM-1ZXX	Remark
JTAG	TMS (Pin4)	TMS	
	TCK (Pin6)	TCK	
	TDI (Pin8)	TDI	
	TDO (Pin10)	TDO	
	RESET_INn (Pin 14)	RESET_Inn via BMC	Also on RST button

MIO Peripherals

Ethernet

The Ethernet port is implemented with a Marvell 88E1512, a resistor field to configure any possible setting of the mode pins, and a low profile Belfuse Mag Jack L829-1J1T-43.
The Primary power supplies are sourced from 3V3_G and 1V8_G, the 1V0 core Voltage is generated by the PHY's internal LDO.

Ethernet Schematic:



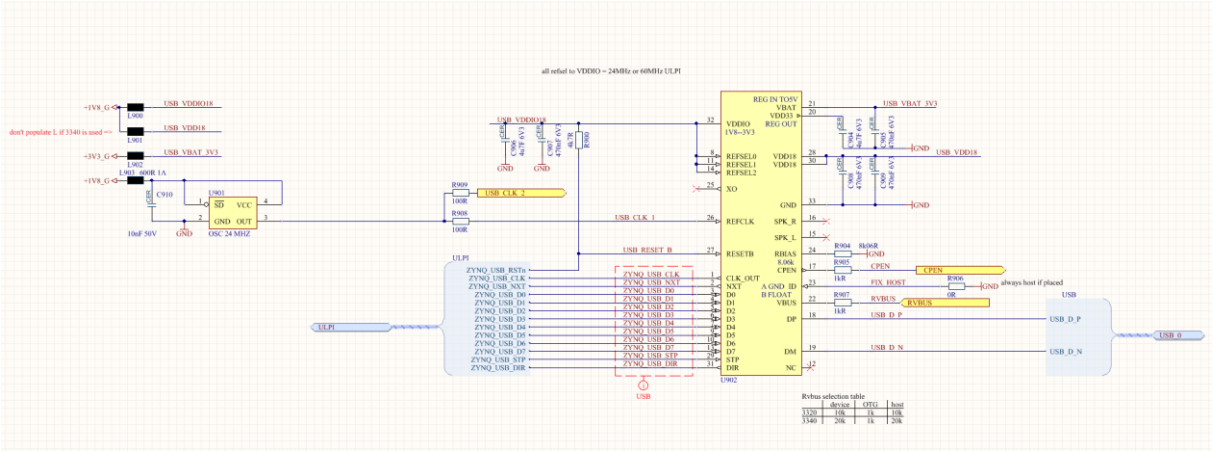
Ethernet Signal Table:

	PIN	GROUP	Signal name	Direction	Remark	I/O Level
ETH	X1_43	MIO_53	ETH_PHY_MDIO	FPGA ⇔ ETH_PHY	Pull up on Carrier	1V8
	X1_45	MIO_52	ETH_PHY_MDC	FPGA => ETH_PHY		1V8
	X1_47	MIO_49	ETH_PHY_RESETn	FPGA => ETH_PHY	Pull up on Carrier	1V8
	X1_77	MIO_16	ETH_TX_CLK	FPGA <= ETH_PHY		1V8
	X1_65	MIO_21	ETH_TX_CTRL	FPGA <= ETH_PHY		1V8
	X1_67	MIO_20	ETH_TX_D3	FPGA => ETH_PHY		1V8
	X1_71	MIO_19	ETH_TX_D2	FPGA => ETH_PHY		1V8
	X1_73	MIO_18	ETH_TX_D1	FPGA => ETH_PHY		1V8
	X1_75	MIO_17	ETH_TX_D0	FPGA => ETH_PHY		1V8
	X1_63	MIO_22	ETH_RX_CLK	FPGA <= ETH_PHY		1V8
	X1_51	MIO_27	ETH_RX_CTRL	FPGA => ETH_PHY		1V8
	X1_53	MIO_26	ETH_RX_D3	FPGA <= ETH_PHY		1V8
	X1_55	MIO_25	ETH_RX_D2	FPGA <= ETH_PHY		1V8
	X1_57	MIO_24	ETH_RX_D1	FPGA <= ETH_PHY		1V8
	X1_61	MIO_23	ETH_RX_D0	FPGA <= ETH_PHY		1V8

USB

The USB interface is implemented with an ULPI connected USB3320C USB PHY chip from SMSC (now Microchip).
R906 forces the port into Host mode. A downstream hub expands the USB connectivity to 4 ports.

USB Schematic:



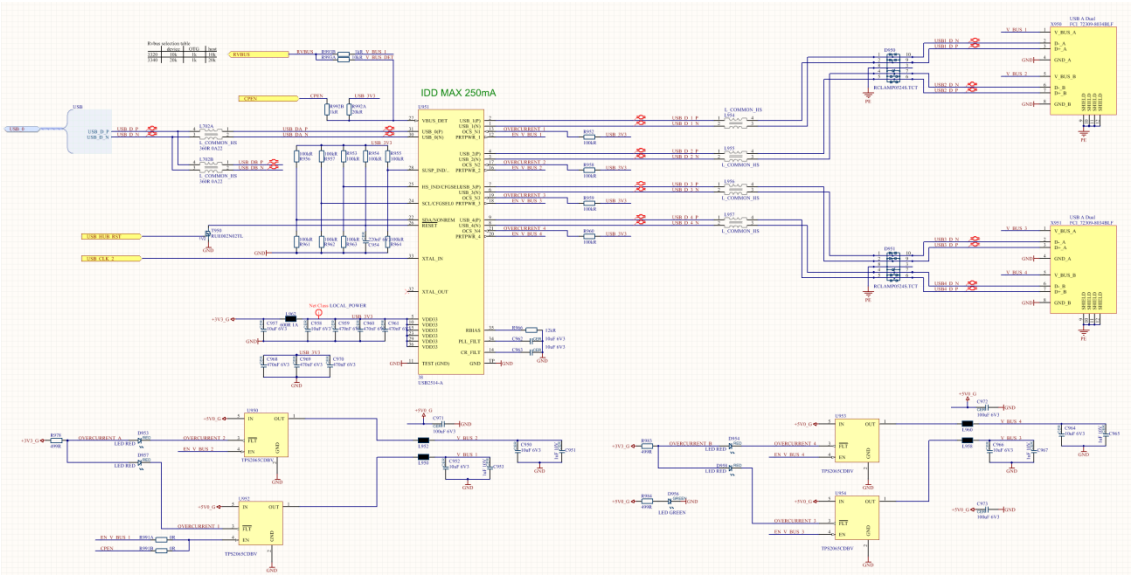
USB Signal Table:

	PIN	MIO	Signal name	Direction	Remark	I/O Level
USB	X1_41	MIO_48	ZYNQ_USB_RST_n	FPGA => USB	Pull up on Carrier	1V8
	X1_52	MIO_36	ZYNQ_USB_CLK	FPGA <= USB		1V8
	X1_38	MIO_31	ZYNQ_USB_NXT	FPGA => USB		1V8
	X1_42	MIO_32	ZYNQ_USB_D0	FPGA <=> USB		1V8
	X1_44	MIO_33	ZYNQ_USB_D1	FPGA <=> USB		1V8
	X1_46	MIO_34	ZYNQ_USB_D2	FPGA <=> USB		1V8
	X1_48	MIO_35	ZYNQ_USB_D3	FPGA <=> USB		1V8
	X1_32	MIO_28	ZYNQ_USB_D4	FPGA <=> USB		1V8
	X1_54	MIO_37	ZYNQ_USB_D5	FPGA <=> USB		1V8
	X1_56	MIO_38	ZYNQ_USB_D6	FPGA <=> USB		1V8
	X1_58	MIO_39	ZYNQ_USB_D7	FPGA <=> USB		1V8
	X1_36	MIO_30	ZYNQ_USB_STP	FPGA => USB		1V8
	X1_34	MIO_29	ZYNQ_USB_DIR	FPGA => USB		1V8

USB HUB

The USB Hub expands the USB port to four interfaces, implemented with standard stacked type A connectors. The 4 USB ports support the easy connection of Keyboard, Mouse, Wi-Fi and a USB drive when the host Module is running Linux.
Over current conditions on the 5V rail will be indicated by a red LED per port pair.

USB HUB Schematic:



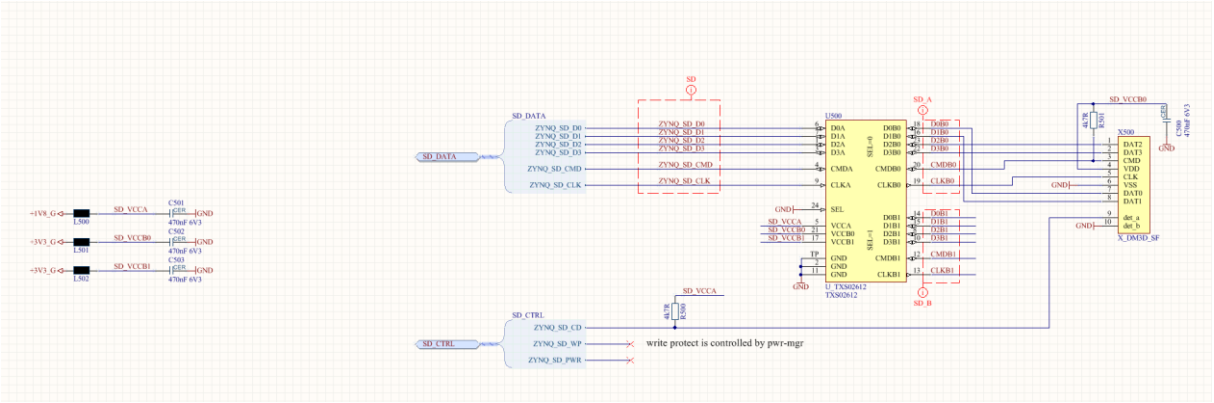
SD

The SD card interface is implemented with a simple buffer, the TXS02612 from TI. While this chip supports the attachment of up to two SD card connectors and a card select pin, only one micro SD card slot is physically implemented and the select pin is tied to GND.

Since the micro SD card does not support a Write protect flag, the write protect function is implemented as a FW option in the power manager uC. The user can activate or de-activate the write protect status of the SD card via the serial console options of the power manager.

The power manager uC also monitors the CD (Card Detect) signal. Depending on the selected boot mode, the module's boot behavior may be influenced by the CD signal.
Boot Option1: Boot and configure from QSPI of Module, regardless of CD status
Boot Option2: Boot and configure from SD card
Boot Option3: Boot and configure from SD card if present, otherwise fall back to QSPI of Module

SD Schematic:



SD Signal Table:

	PIN	MIO	Signal name	Direction	Remark	I/O Level
SD	X1_66	MIO_42	ZYNQ_SD_D0	FPGA <=> SD		1V8
	X1_68	MIO_43	ZYNQ_SD_D1	FPGA <=> SD		1V8
	X1_72	MIO_44	ZYNQ_SD_D2	FPGA <=> SD		1V8
	X1_74	MIO_45	ZYNQ_SD_D3	FPGA <=> SD		1V8
	X1_64	MIO_41	ZYNQ_SD_CMD	FPGA => SD		1V8
	X1_62	MIO_40	ZYNQ_SD_CLK	FPGA => SD		1V8
	X1_76	MIO_46	ZYNQ_SD_CD	FPGA <=PMGR <= SD	PMGR monitors CD signal	1V8
	X1_78	MIO_47	ZYNQ_SD_WP	FPGA <= PMGR	WP via FW setting (user access)	1V8

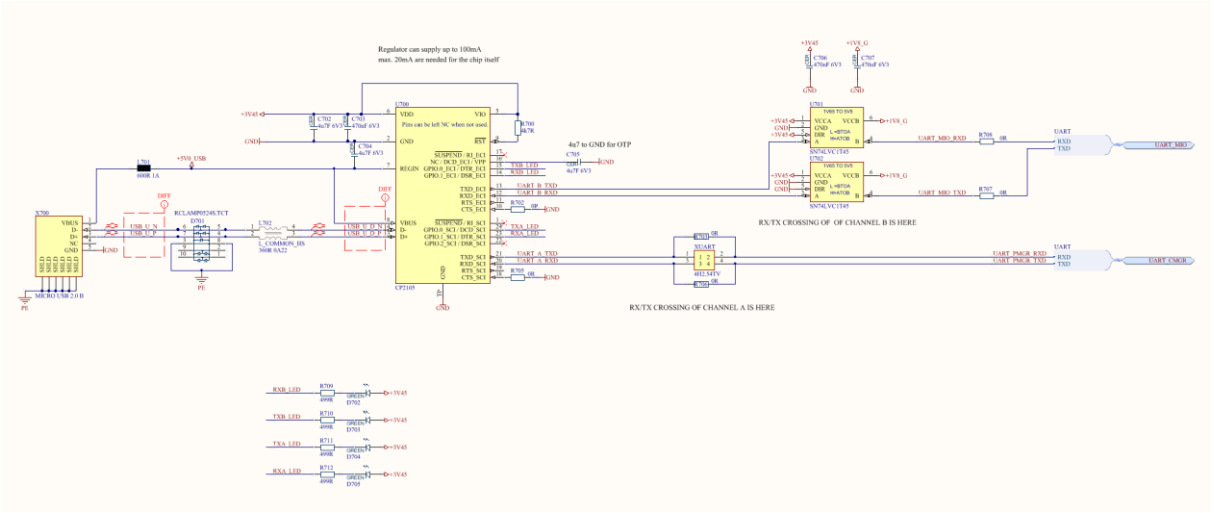
UART to USB Bridge

The KRC1711 features a dual channel Silabs UART to USB Bridge (CP2105). One channel's RX and TX signals are connected to UART0 of the Zynq PS.

The second channel is connected to the power manager control console. The connection is completed by two 0R resistors which may be removed to enable re-routing this UART channel to a PL I/O bank or other circuit. Keep in mind that the UART to USB bridge I/O levels are slightly above 3V3, so if the UART is patched to a PL bank, **the bank must be operated with 3V3 I/O levels** or a level converter buffer must be inserted.

The 5V USB supply that is provided by the host PC is also used to power the LDO of the power manager. This allows interaction with the power manager even if no primary power supply (12V) is connected to the KRC1711. This feature allows the user to configure settings without the need for a power supply.

UART to USB Bridge Schematic:



UART MIO Signal Table:

	PIN	MIO	Signal name	Direction	Remark	I/O Level
UART	X1_37	MIO_50	UART_MIO_RXD	FPGA_PS <= CP2105	Via voltage buffer	1V8
	X1_35	MIO_51	UART_MIO_TXD	FPGA_PS => CP2105	Via voltage buffer	1V8

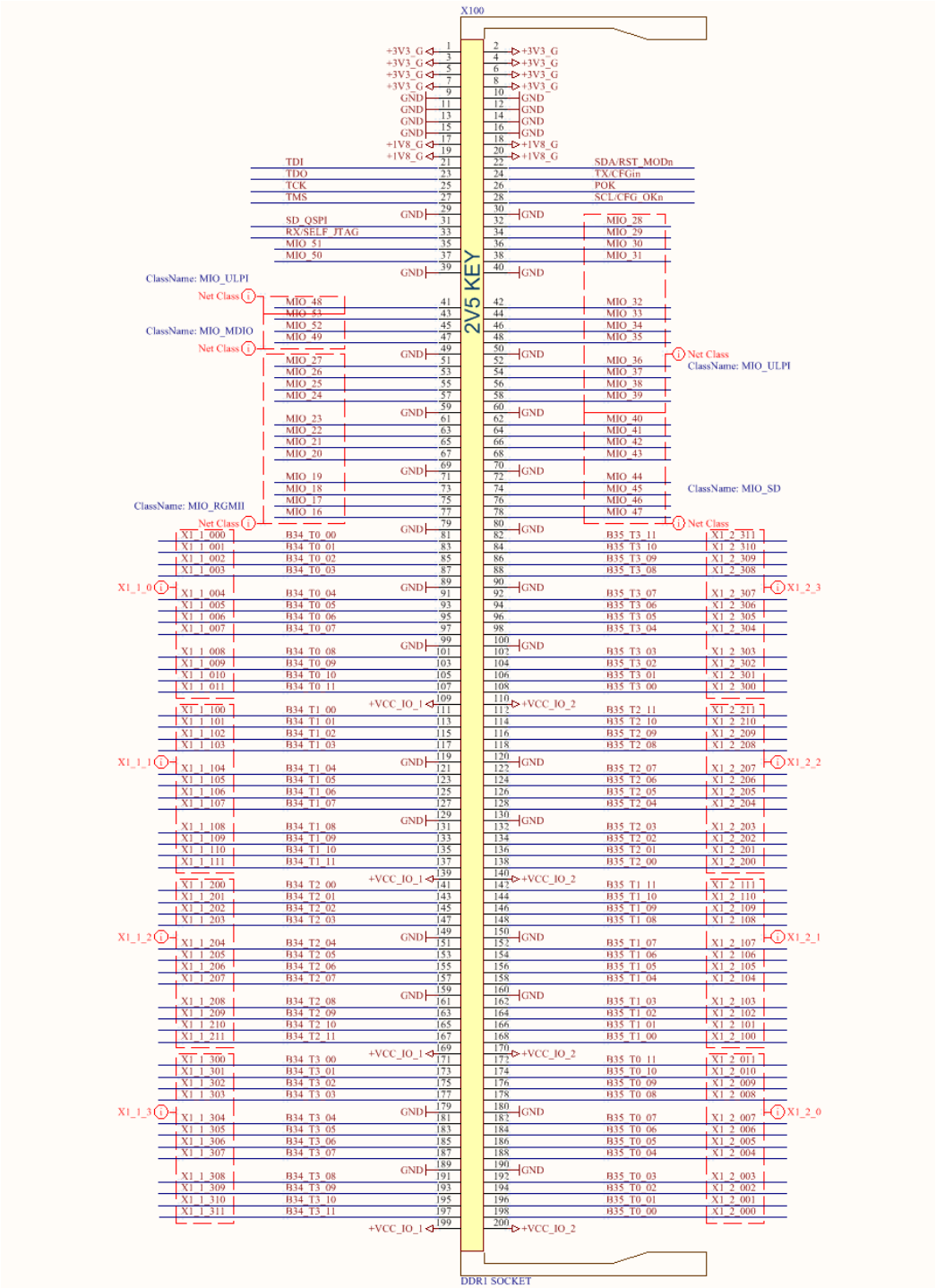
UART PMGR Signal Table:

	PIN PMGR		Signal name	Direction	Remark	I/O Level
UART	21	RX	UART_PMGR_RXD	PMGR <= CP2105	No buffer	3V3
	22	TX	UART_PMGR_TXD	PMGR => CP2105	No buffer	3V3

PL IO

All PL I/O Banks support a range of I/O voltages, two of which are provided by the on-board regulators; others may be added by the user.
Use the 5V0 on-board regulator as the source for any additional I/O voltage regulator.

Supported/**Provided** I/O voltages are: 1V5, **1V8**, 2V5 and **3V3.**
I/O voltages below 1V5 are NOT supported by the KRM-1Z7xxx modules as the I/O voltage is isolated by a high side P-FET switch which is only active after the FPGA has been configured or the modules power sub system reports power OK. Gate Voltages that do not at least reach 1V5 do not turn the P-FET on sufficiently; therefore 1V35 I/O voltages or below, cannot be used reliably.

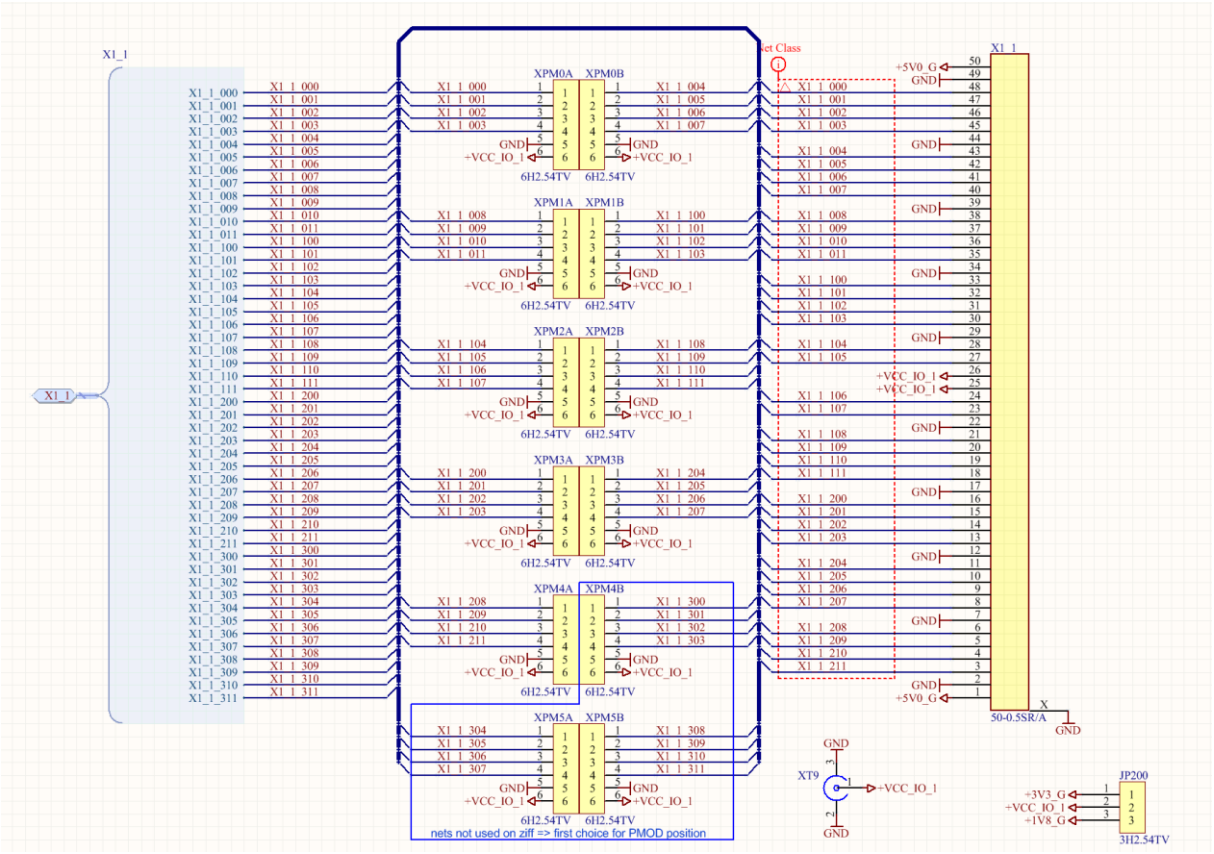


PL BANK X1_1

The PL Bank that is mapped to X1_1 is one of the two general purpose PL I/O banks. Byte Lanes 0-2 are mapped to a 50 pin Ziff header which supports standard KR peripherals. Byte Lane 3 is available on the 2.54mm raster solder field.

The Bank's I/O Voltage is selected by populating JP200 with a jumper to 1V8 or 3V3. If other operating voltages are desired, the target supply voltage must be jumped to the center pin with a wire from a suitable regulator.

PL BANK X1_1 Schematic:



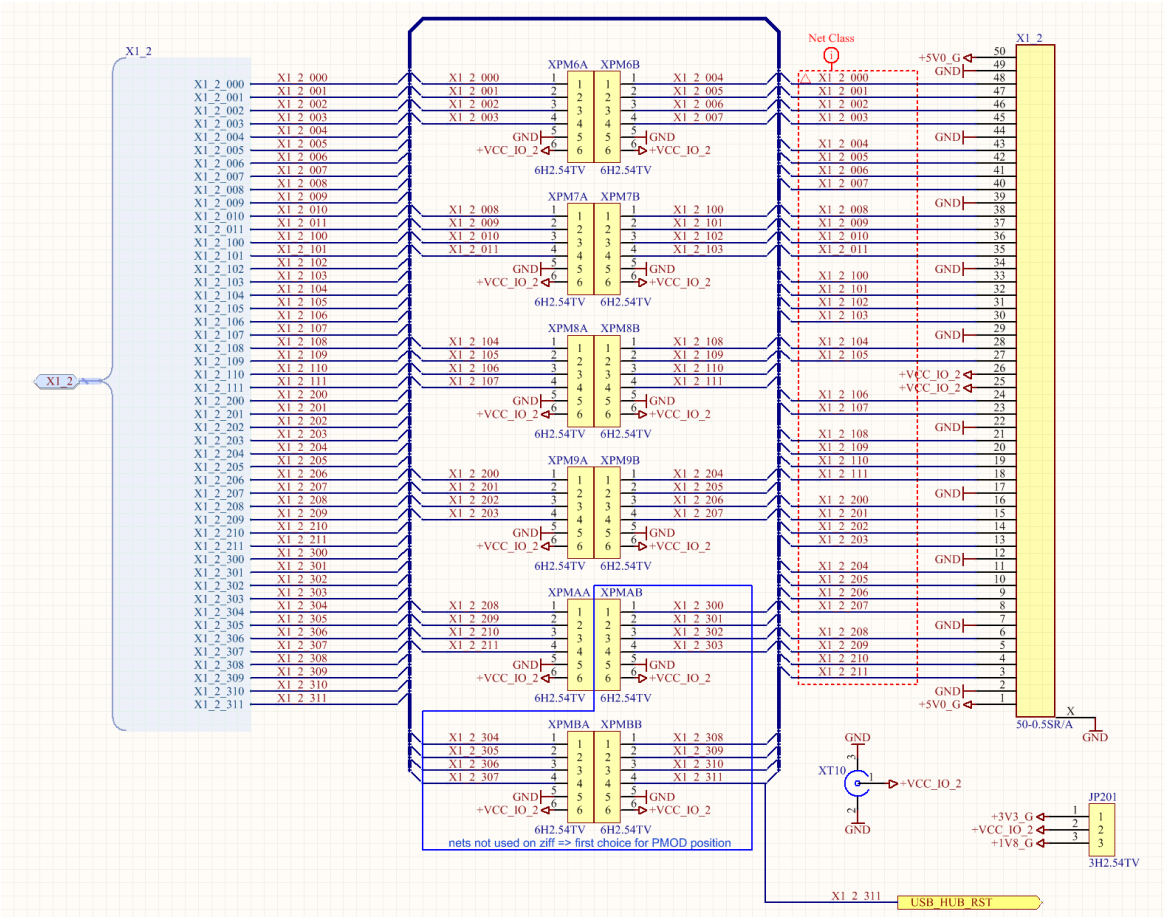
PL BANK X1_2

The PL Bank that is mapped to X1_2 is one of the two general purpose PL I/O banks. Byte Lanes 0-2 are mapped to a 50 pin Ziff header which supports standard KR peripherals. Byte Lane 3 is available on the 2.54mm raster solder field.

The Bank's I/O Voltage is selected by populating JP201 with a jumper to 1V8 or 3V3. If other operating voltages are desired, the target supply voltage must be jumped to the center pin with a wire from a suitable regulator.

Please note that signal X1_2_311 is used to drive the reset signal of the USB hub.

PL BANK X1_2 Schematic:



Compliance

All KRM modules and KRC Carriers are ROHSII and REACH compliant. For further details, customers may request the current declaration of conformity by emailing office@knowres.ch.
All KRM Modules are manufactured with UL94V-0 flammability rated PCBs with an IPC Class2 quality rating.

Electrical Specification

ESD

KRM Modules are sensitive to electrostatic discharge and must be handled with proper ESD precautions.

Absolute Maximum Ratings[i]

Symbol	Description	Min	Max
POWER_IN	Global power in	-0V5	16V0
VCCO_34/35	HR Bank I/O power supply	-0V5	3V6
PL_IO_HR	HR Bank I/O signal levels	-0V5	3V6

Recommended Operating conditions

Symbol	Description	Min	Typ	Max
POWER_IN	Global power in	9V0	12V0	14V0
VCCO_34/35	HR Bank I/O power supply	3V2	3V3	3V4
PL_IO_HR	HR Bank I/O signal levels	-0V2	--	VCCO + 0V2

Thermal specification

Absolute Maximum Ratings[ii]

Symbol	Description	Min	Max
Delta T	Max temperature change per second while operating	--	+/-1°C/sec
TSTG	Storage temperature ambient un-powered	-40°C	+125°C

Recommended Operating Conditions

Symbol	Description	Min	Typ	Max
Tj C	Operating Junction temperature of FPGA for commercial grade	0°C	--	+70°C
Tj I	Operating Junction temperature of FPGA for industrial grade	-40°C	--	+85°C
Delta T	Allowed temperature change per second while operating	--	--	+/-0.5°C/sec

[i] Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied.
Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect module reliability
[ii] Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied.

Errata

No known errata at the time of writing