KNOWLEDGE RESOURCES
Switzerland GmbH

KRC3701-CARRIER

Data sheet V1.2

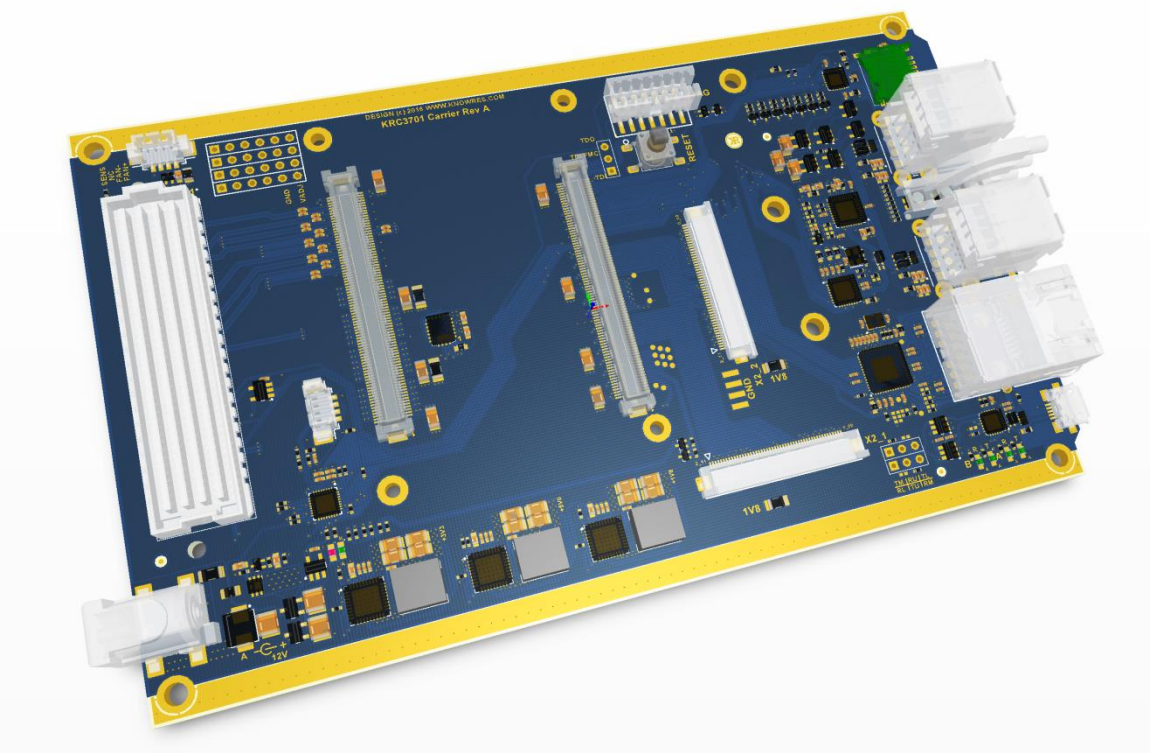

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Table of Contents

Revision History

Date	Document revision	HW revision	Changes
Sept 27th 2016	0.1	REV A	Import from KRC3600
Sept 27th 2016	1.0	REV A	Changes to KRC3701 First public release
Oct. 31st 2016	1.1	REV A	Correction in FMC signal table on page 18 LA06_P/N corrected to C10/11 (was false as C11/12)
Jul.19th 2017	1.2	REV A	Correction signal table on page 24 MGT_RX04 – 07 had a 2 pin offset in numbering Updated Company address on front page

Disclaimer

All provided data is for information purposes only and not guaranteed for legal purposes.

Information has been carefully checked and is believed to be accurate;

However, no responsibility is assumed for inaccuracies.

Specifications are subject to change without notice.

Trademark Acknowledgement:

Brand and product names are trademarks or registered trademarks of their respective owners.

Assumptions

The reader is familiar with Xilinx FPGA and SoC components and the related terminology in common use.

Acronyms

BMC:	Board Management Controller
FU:	Future Use
KR:	Knowledge Resources GmbH
MGT:	Multi Gigabit Transceiver
NA:	Not Applicable
PL:	Programmable Logic
PS:	Processing Subsystem
SoC:	System on Chip
SoM:	System on Module
uC:	Microcontroller

Reference documents

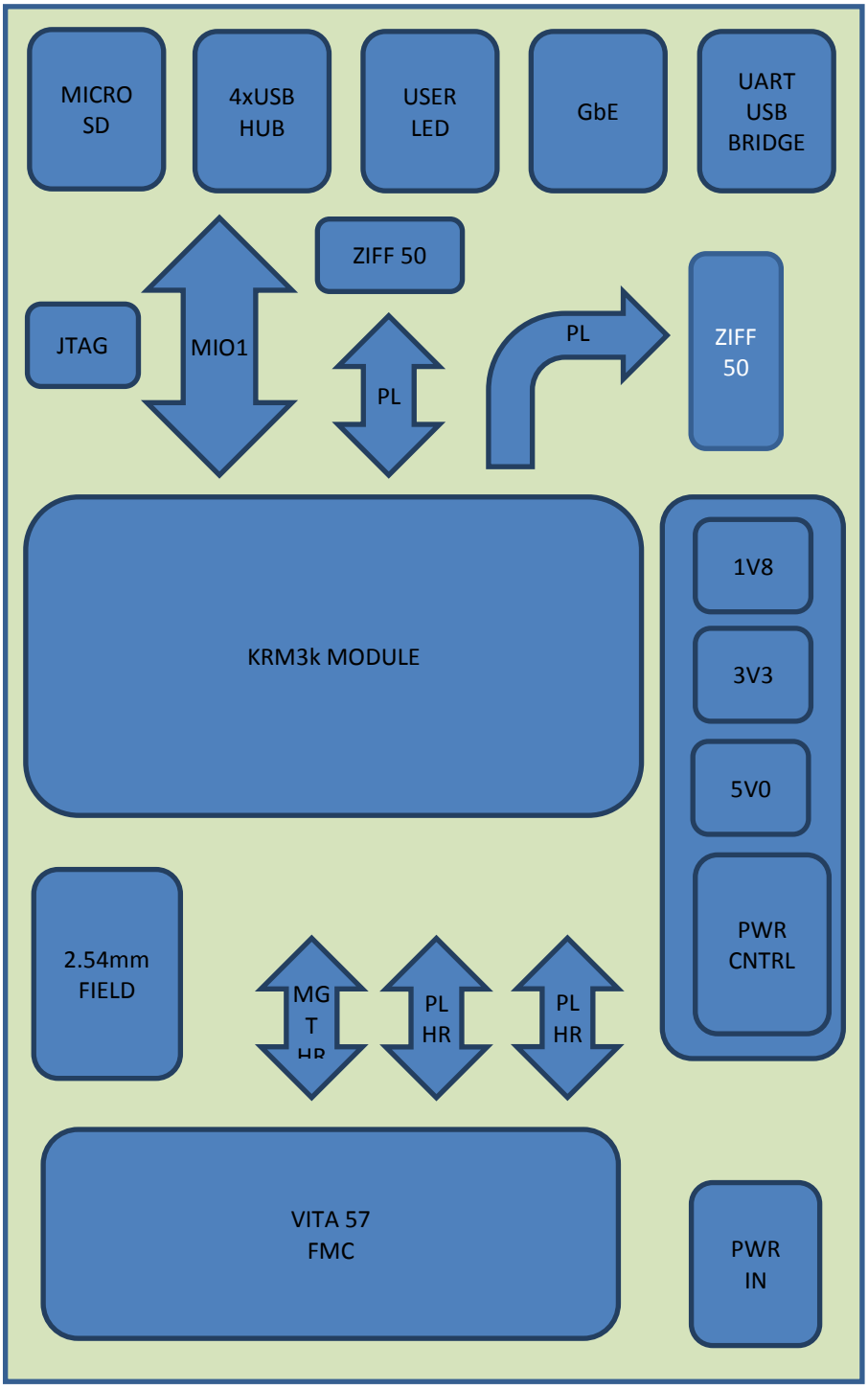
ZYNQ all programmable SoC, Xilinx, www.xilinx.com
MARVELL Ethernet PHY[i]: http://www.marvell.com/transceivers/fast-ethernet-phy/
SMSC USB PHY: http://ww1.microchip.com/downloads/en/DeviceDoc/3320.pdf
Silabs UART to USB: http://www.silabs.com/products/interface/usbtouart/Pages/usb-to-uart-bridge.aspx
INTERSIL Regulator: http://www.intersil.com/content/dam/Intersil/documents/zl21/zl2102.pdf
LANSING enclosure: http://www.lansing-enclosures.com/main/micropak/c-style/index.html

[i] Marvell requires registration and NDA on order to grant access to the datasheet

Introduction

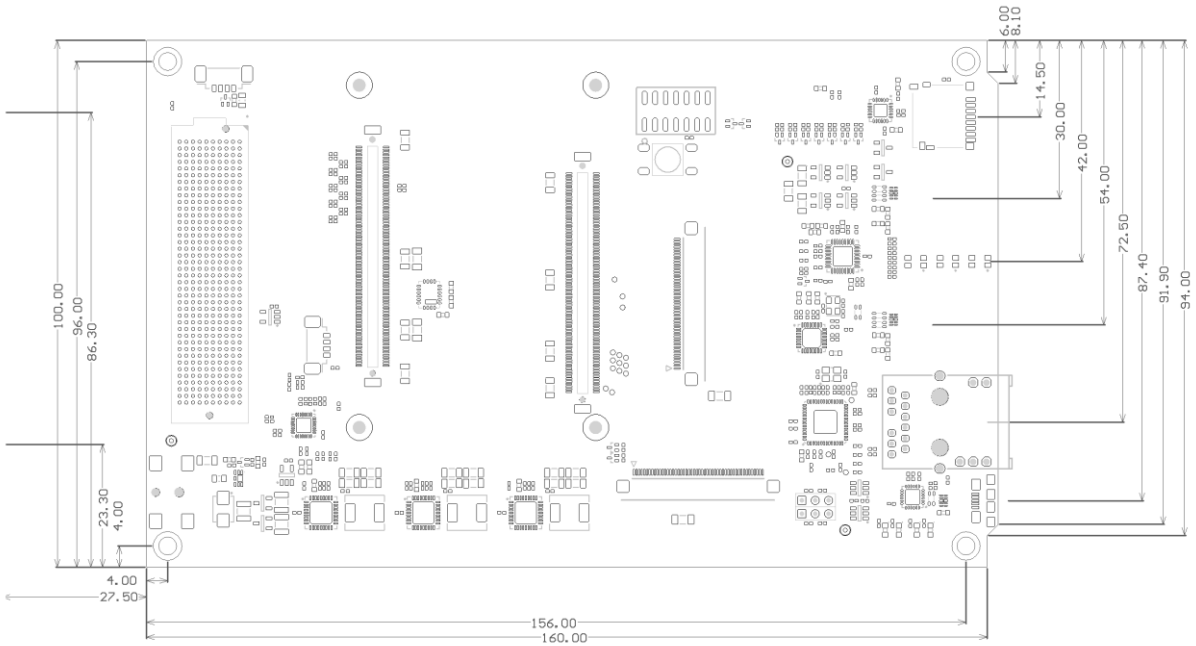
With the KRC3701, Knowledge Resources provides a highly flexible and cost-efficient evaluation board for embedded systems prototyping with KRM-3Z7xxx family modules. The carrier board offers all of the essential infrastructure elements that are required to operate a KRM-3Z7xxx family module. Furthermore, the PL ports are readily accessible via 50 pin Ziff expansion connectors, 2.54mm sockets and a VITA57 compliant FMC connector. MGT lanes are routed to the first 8 positions of the FMC connector.

The carrier has a Euro-card form factor of 100x160mm and fits into a Lansing “micropack c-style” Enclosure, thereby facilitating the fabrication of complete small run projects without significant investments into custom Enclosures.



Board dimensions

(in mm)



- Altium PCB and Schematic templates are available

Features

Overview

- Accepts KRM-3Z7xxx series modules
- Dual UART to USB bridge
- 1 x Micro SD Slot
- 4 x USB port (via 4 port hub)
- 1 x Gb Ethernet Port
- 2 x 50Pin Ziff Headers (one per PL Bank)
- 1 x FMC with 8 MGT lanes and 72 I/O ports
- 3 User LED (RGB) with light pipes to rear panel
- JTAG debug port
- Single 12V DC supply input 2.1mm by 5.5mm barrel jack
- 12V FAN connector
- Configurable power manager

Power supply

Normal operating conditions

The KRC3701 is designed to accept 12V DC. In order to fully support the range of modules and daughter cards that can be paired with the KRC3701 a 12V power supply able to source at least 3A is recommended.

The KRC3701 generates three “global” Voltages: 5V, 3V3 and 1V8. All are capable of sourcing up to 6A. The inputs of the regulators are globally fused. The power OK signals are used to activate power good indicators.

The 3V3 Supply powers the KRM-3Z7XXX Module and several I/O peripheral circuits (such as the SD card socket).

The 1V8 supply powers a multitude of peripherals such as the USB Phy, Ethernet Phy, and parts of the SD card interface chip. 1V8 supply is the default bank I/O supply voltage for each of the module’s two generic PL I/O banks.

The PL banks that drive the FMC connector are powered by a dedicated, dynamically adjustable DC/DC converter which provides the V-ADJ voltage to the FMC connector. This voltage setting can be changed via serial commands on the power manager console. Once changed, the voltage setting may be stored in the power manager's non-volatile memory.

The KRC3701s input is reverse polarity, over-voltage and under-voltage protected.
- Reverse polarity will trip a self-healing fuse.
- The power manager monitors the input voltage and prevents the 12V soft start form being enabled if the input voltage exceeds 13V DC. This ensures that the following regulator’s input voltage limit is not exceeded. The power manager also monitors the supply after power up and will initiate an emergency shut down if the input voltage rises above 13V. The input overvoltage protection will fail if exposed to input voltages above 20V. This feature will most likely prevent the KRC3701 from operating on an automotive DC supply which may exceed 14V when the alternator is charging the on-board battery.
- The power manager also monitors the input voltage for an under voltage condition. It prevents power up if the voltage is below 11V DC, and initiates power down if the input voltage falls below 10V DC.

	PARAMETER	MIN	NOMINAL	MAX
PWR OPERATING CONDITIONS	V-IN	10V DC	12V DC	13V DC
	UVLO turn on limit	11V DC		
	UVLO turn off limit			10V DC
	OV power up limit	13V DC		
	I MAX continuous		4A	

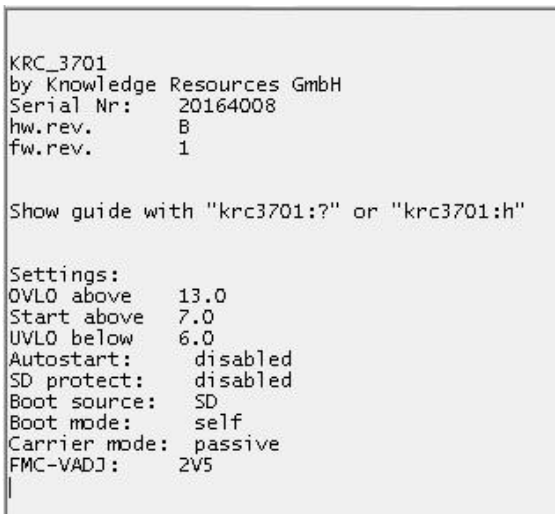
Factory settings

In its factory configuration, the KRC3701 is configured to power up once a valid 12V supply is detected. This may be changed to a mode that requires a power up command on the power manager's serial console.

	PARMETER	DEFAULT	OPTION	REMARK
FACTORY DEFAULTS	Auto power on	ON	OFF	Within valid V-in range
	V ADJ	1V8	2V5,3V3	
	Baud rate	115200	N/A	

Control console

When the KRC3701 UART to USB console port is connected to a host PC, two virtual COM ports will be activated. The COM port numbers depend on the host system. One of the ports is connected to the PS debug console, the other to the BMC. Configure a terminal program to 115200 Baud, 8N1 and then connect the host to the carrier, the following welcome message will be received:



Every command to the KRC3701 must be preceded by "KRC3701:"
Use the command "KRC3701:?" For a list of supported commands.

Reset

The KRM-3Z7xxx modules generate their own on board power on reset. A user reset button for the PS of the Zynq on a KRM-3Z7xxx module is available.
The reset signal is also routed to the JTAG connector therefore enabling full debug support for the ARM cores.
The Reset signal is buffered by the BMC, which allows issuing a reset of the module by the BMC and creates options for future generation Modules that are beyond the scope of this datasheet.

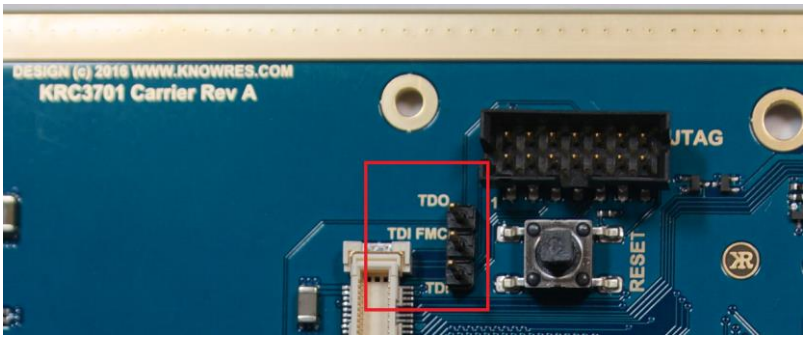
JTAG

The JTAG Jumper next to the module allows bypassing the FMC JTAG chain (default when no FMC module is present) or bypassing the KRM-3Z7xxx module if no module is present. If both an FMC module and a KRM-3Z7xxx module are plugged in, the jumper MUST be removed.

JTAG Signals:

	PGM HEADER	KRM-3ZXX	FMC	JMPR_LABEL	Remark
JTAG	TMS (Pin4)	TMS	TMS		
	TCK (Pin6)	TCK	TCK		Buffered to FMC
	TDI (Pin8)			TDI	
		TDO	TDI FMC	TDI_FMC	
	TDO (Pin10)		TDO	TDO	
	RESET_INn (Pin 14)	RESET_Inn via BMC	TRST_L		Also on RST button

JTAG Jumper:

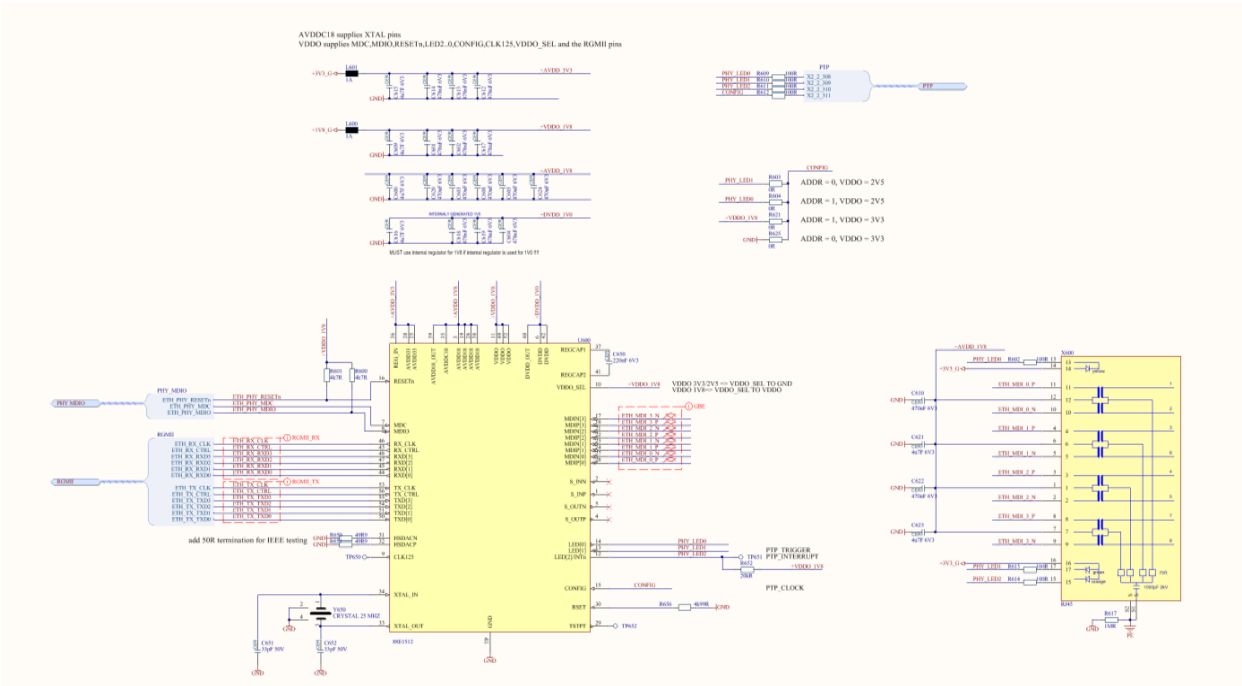


MIO Peripherals

Ethernet

The Ethernet port is implemented with a Marvell 88E1512, a resistor field to configure any possible setting of the mode pins, and a low profile Belfuse Mag Jack L829-1J1T-43.
The resistor field is populated to put the Phy on Address 0, The Primary power supply is sourced from 3V3_G, the I/O bank from 1V8_G. The 1V0 core Voltage and 1V8 AVDD is generated by the PHY's internal LDOs.

Ethernet Schematic:



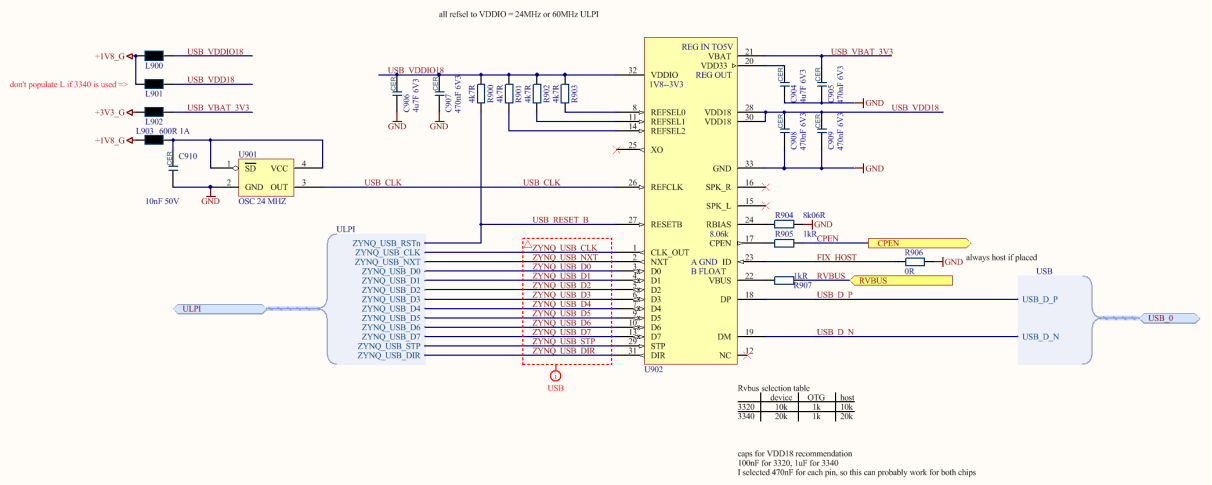
Ethernet Signal Table:

	PIN	GROUP	Signal name	Direction	Remark	I/O Level
ETH	X2_163	MIO_53	ETH_PHY_MDIO	FPGA ⇔ MDIO	Pull up on Carrier	1V8
	X2_164	MIO_52	ETH_PHY_MDC	FPGA => MDIO		1V8
	X2_159	MIO_49	ETH_PHY_RESETn	FPGA => MDIO	Pull up on Carrier	1V8
	X2_122	MIO_16	ETH_TX_CLK	FPGA <= MDIO		1V8
	X2_127	MIO_21	ETH_TX_CTRL	FPGA <= MDIO		1V8
	X2_128	MIO_20	ETH_TX_D3	FPGA => MDIO		1V8
	X2_123	MIO_19	ETH_TX_D2	FPGA => MDIO		1V8
	X2_124	MIO_18	ETH_TX_D1	FPGA => MDIO		1V8
	X2_121	MIO_17	ETH_TX_D0	FPGA => MDIO		1V8
	X2_130	MIO_22	ETH_RX_CLK	FPGA <= MDIO		1V8
	X2_133	MIO_27	ETH_RX_CTRL	FPGA => MDIO		1V8
	X2_134	MIO_26	ETH_RX_D3	FPGA <= MDIO		1V8
	X2_131	MIO_25	ETH_RX_D2	FPGA <= MDIO		1V8
	X2_132	MIO_24	ETH_RX_D1	FPGA <= MDIO		1V8
	X2_129	MIO_23	ETH_RX_D0	FPGA <= MDIO		1V8

USB

The USB interface is implemented with a ULPI connected USB3320C USB PHY chip from SMSC (now Microchip). R906 forces the port into Host mode. A downstream hub expands the USB connectivity to 4 ports.

USB Schematic:



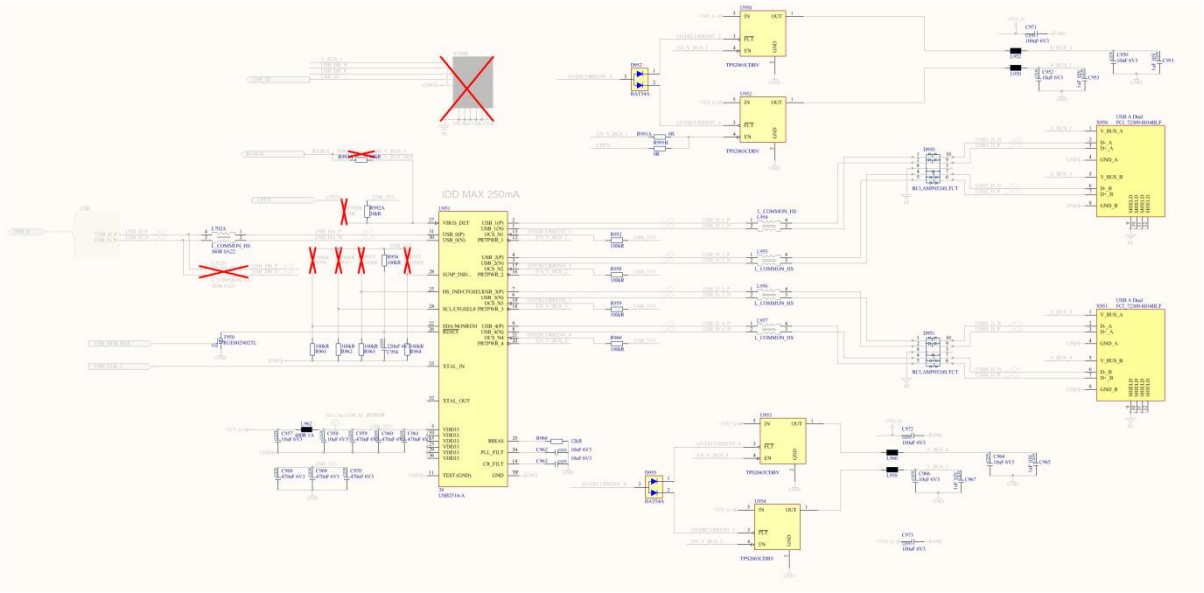
USB Signal Table:

	PIN X2	MIO	Signal name	Direction	Remark	I/O Level
USB	X2_160	MIO_48	ZYNQ_USB_RST_n	FPGA => USB	Pull up on Carrier	1V8
	X2_146	MIO_36	ZYNQ_USB_CLK	FPGA <= USB		1V8
	X2_139	MIO_31	ZYNQ_USB_NXT	FPGA => USB		1V8
	X2_142	MIO_32	ZYNQ_USB_D0	FPGA <=> USB		1V8
	X2_141	MIO_33	ZYNQ_USB_D1	FPGA <=> USB		1V8
	X2_144	MIO_34	ZYNQ_USB_D2	FPGA <=> USB		1V8
	X2_143	MIO_35	ZYNQ_USB_D3	FPGA <=> USB		1V8
	X2_136	MIO_28	ZYNQ_USB_D4	FPGA <=> USB		1V8
	X2_145	MIO_37	ZYNQ_USB_D5	FPGA <=> USB		1V8
	X2_148	MIO_38	ZYNQ_USB_D6	FPGA <=> USB		1V8
	X2_147	MIO_39	ZYNQ_USB_D7	FPGA <=> USB		1V8
	X2_140	MIO_30	ZYNQ_USB_STP	FPGA => USB		1V8
	X2_135	MIO_29	ZYNQ_USB_DIR	FPGA => USB		1V8

USB HUB

The USB Hub expands the USB port to four interfaces, implemented with standard stacked type A connectors. The 4 USB ports support the easy connection of Keyboard, Mouse, Wi-Fi and a USB drive when the host Module is running Linux.
Optionally the HUB can be bypassed on the shaded out micro USB connector activated as a USB OTG interface

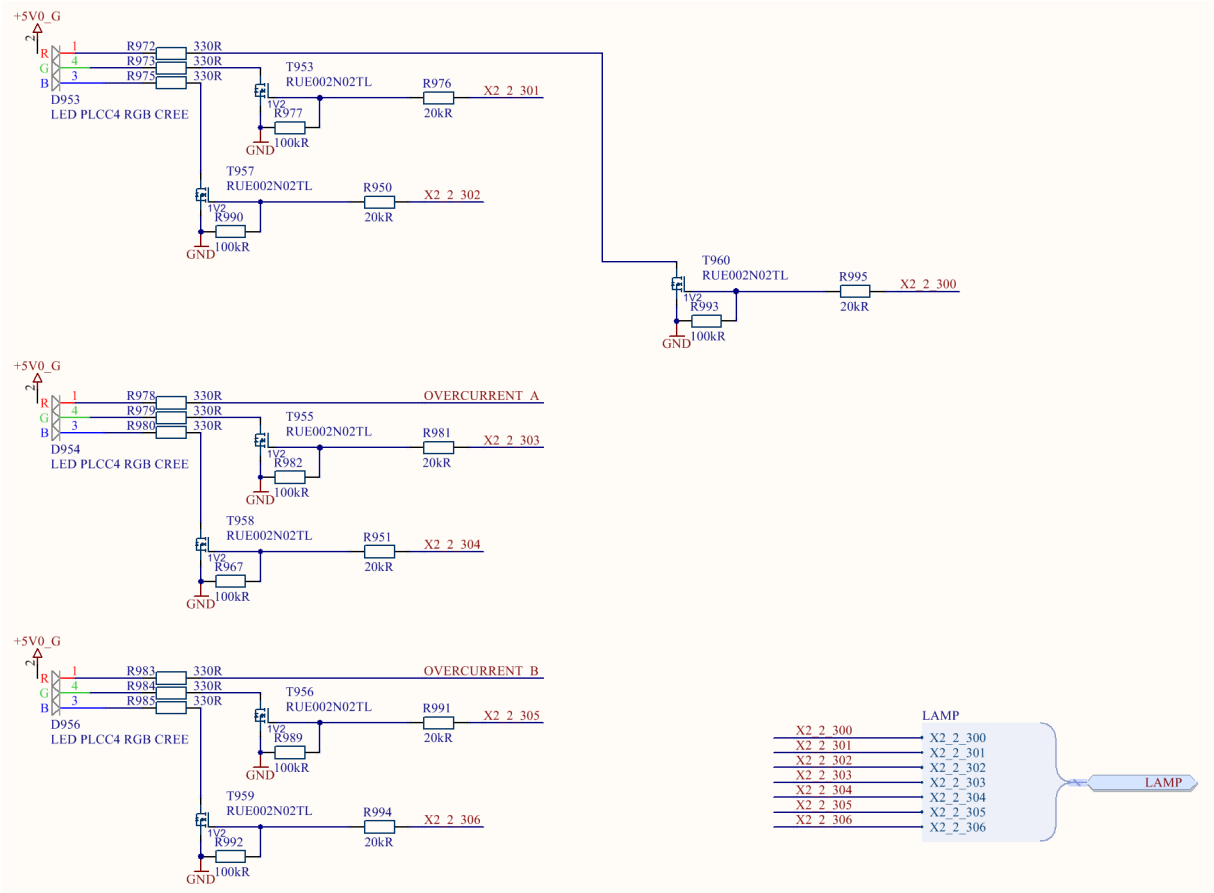
USB HUB Schematic:



USER LED

The KRC3701 features 3 RGB LEDs. The red channels of LED 954 and LED956 are used to indicate an overcurrent event on the USB ports. All other channels are available as User LEDs on a range of Signals on X2 of the SoC module.

USER LED Schematic:



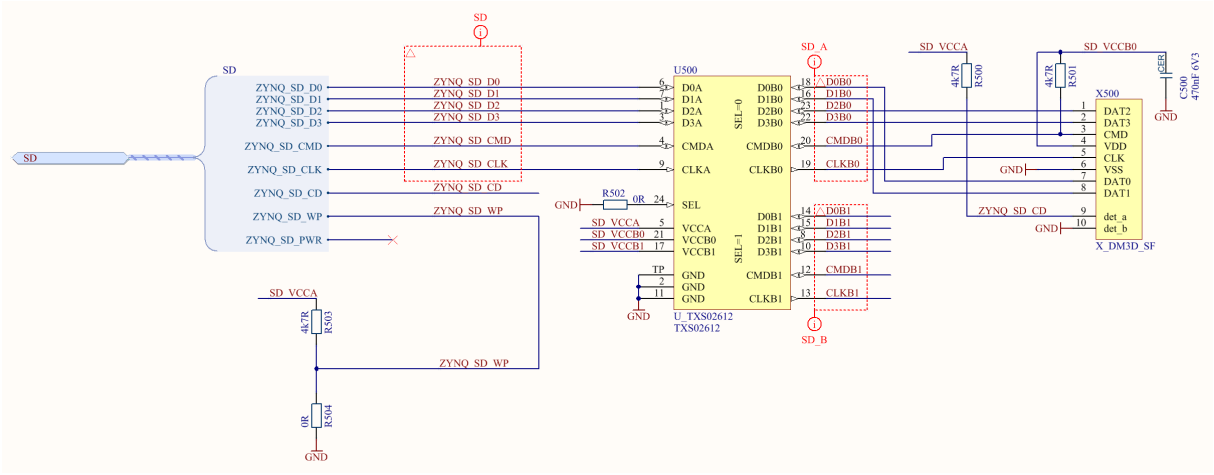
USER LED Signal Table:

	PIN X2	BANK	Signal name	Direction	Remark	I/O Level
USER LED	X2_83	X2_2	X2_2_300	FPGA => USER LED	Red	1V8
	X2_81	X2_2	X2_2_301	FPGA => USER LED	Green	1V8
	X2_79	X2_2	X2_2_302	FPGA => USER LED	Blue	1V8
	X2_77	X2_2	X2_2_303	FPGA => USER LED	Green	1V8
	X2_75	X2_2	X2_2_304	FPGA => USER LED	Blue	1V8
	X2_73	X2_2	X2_2_305	FPGA => USER LED	Green	1V8
	X2_71	X2_2	X2_2_306	FPGA => USER LED	Blue	1V8

SD

The SD card interface is implemented with a simple buffer, the TXS02612 from TI. While this chip supports the attachment of up to two SD card connectors and a card select pin, only one micro SD card slot is physically implemented and the select pin is tied to low with a 0R resistor.
Since the micro SD card does not support a Write protect flag, the write protect function is implemented as a resistor solder option on the carrier. WP is off by default but can be set by moving a resistor.

SD Schematic:



SD Signal Table:

	PIN X2	MIO	Signal name	Direction	Remark	I/O Level
SD	X2_152	MIO_42	ZYNQ_SD_D0	FPGA <=> SD		1V8
	X2_151	MIO_43	ZYNQ_SD_D1	FPGA <=> SD		1V8
	X2_156	MIO_44	ZYNQ_SD_D2	FPGA <=> SD		1V8
	X2_155	MIO_45	ZYNQ_SD_D3	FPGA <=> SD		1V8
	X2_149	MIO_41	ZYNQ_SD_CMD	FPGA => SD		1V8
	X2_150	MIO_40	ZYNQ_SD_CLK	FPGA => SD		1V8
	X2_158	MIO_46	ZYNQ_SD_CD	FPGA <= SD		1V8
	X2_157	MIO_47	ZYNQ_SD_WP	FPGA <= SD	Resistor on Carrier not on connector	1V8

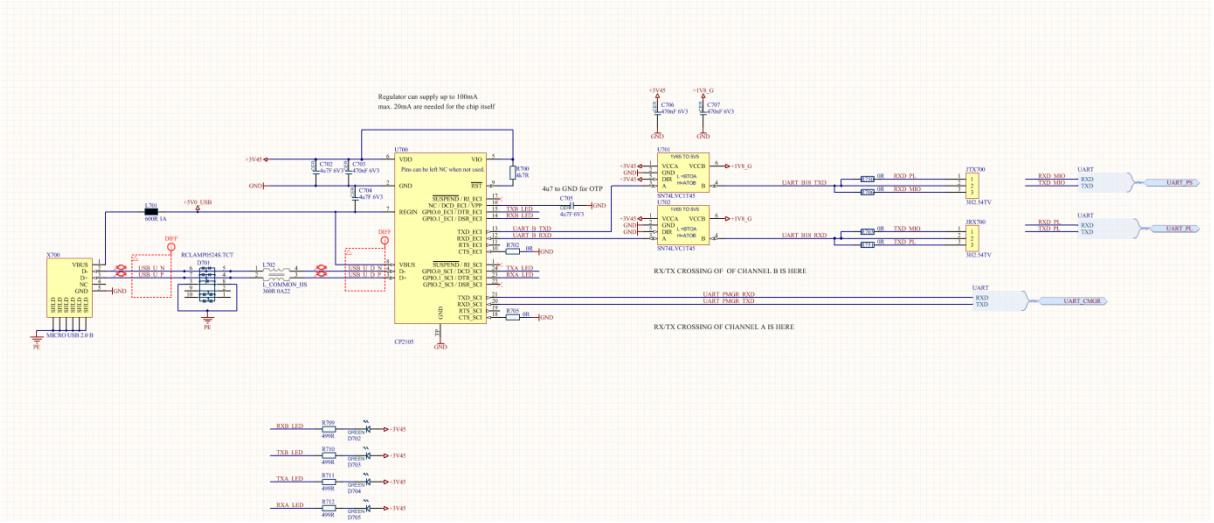
UART to USB Bridge

The KRC3701 features a dual channel Silabs UART to USB Bridge. One channel's RX and TX signals are connected either to UART0 of the Zynq PS or two PL pins. In the default configuration, the UART to USB Bridge is connected to the PS UART via 0-Ohm resistors. This configuration may be changed by unsoldering th e0Ohm resistors and adding pin headers and jumpers or by fitting 0Ohm resistors in the PL link position

The second channel is permanently connected to the UART of the BMC (Board Management Controller). The BMC UART interface provides access to board settings and status information. Please consult the QSG (Quick Start Guide) of the KRC3701 for protocol details and firmware options.

The 5V USB supply that is provided by the host PC is also used to power the LDO of the power manager. This allows interaction with the power manager even if no primary power supply (12V) is connected to the KRC3701. This feature allows the user to configure settings without the need for a power supply.

UART to USB Bridge Schematic:



UART MIO Signal Table:

	PIN X2	MIO	Signal name	Direction	Remark	I/O Level
UART	X2_162	MIO_50	UART_MIO_RXD	FPGA_PS <= CP2105	Via voltage buffer	1V8
	X2_161	MIO_51	UART_MIO_TXD	FPGA_PS => CP2105	Via voltage buffer	1V8

UART PMGR Signal Table:

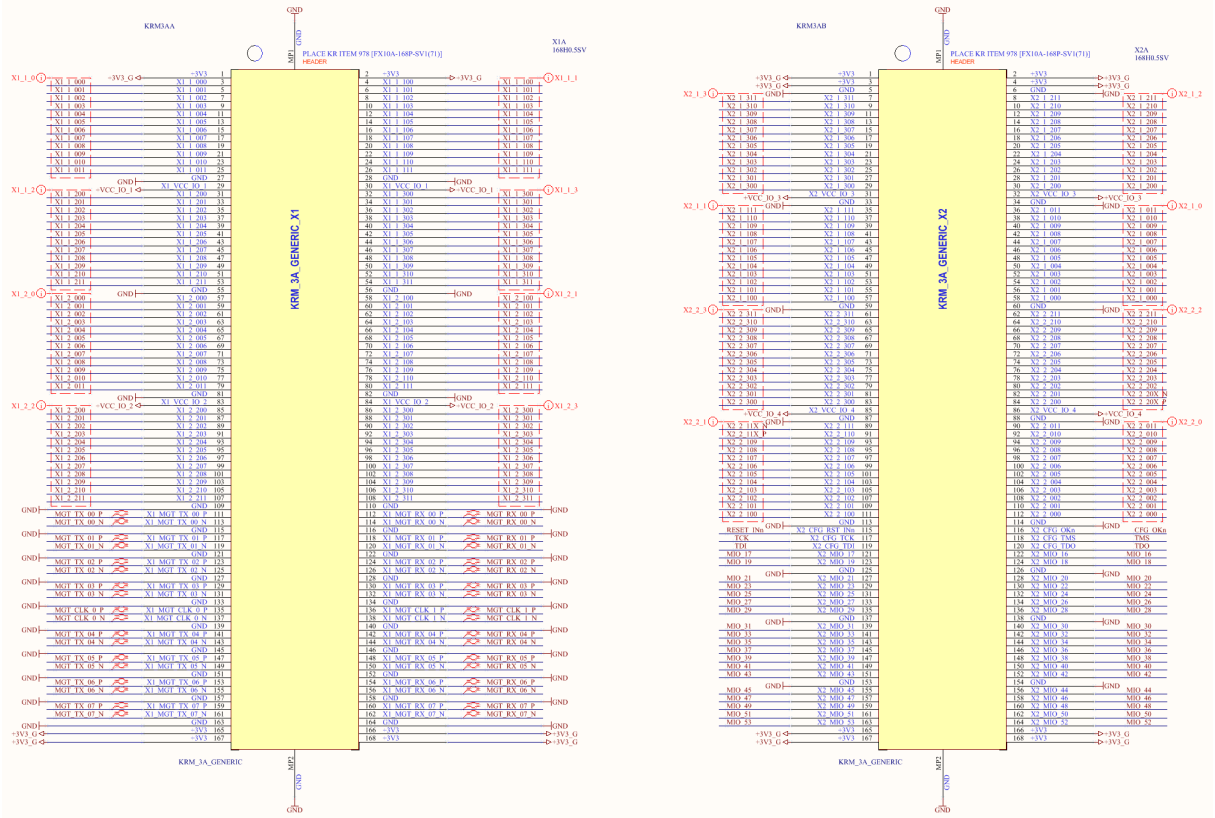
	PIN PMGR		Signal name	Direction	Remark	I/O Level
UART	28	RX	UART_PMGR_RXD	PMGR <= CP2105	No buffer	3V3
	28	TX	UART_PMGR_TXD	PMGR => CP2105	No buffer	3V3

UART FABRIC Signal Table:

	PIN X2	KRM_3A	Signal name	Direction	Remark	I/O Level
UART	X2_7	X2_1_311	UART_FAB_RXD	FPGA_PL <= CP2105	Via voltage buffer	1V8-3V3
	X2_11	X2_1_310	UART_FAB_TXD	FPGA_PL => CP2105	Via voltage buffer	1V8-3V3

PL IO

All PL I/O Banks support multiple I/O voltages, 2 of which are provided by the on-board regulators; others may be added by the user. Use the 5V0 on-board regulator as the source for any additional I/O voltage regulator.
Supported/**Provided** I/O voltages are: 1V35, 1V5, **1V8**, 2V5 and **3V3.**
I/O voltages below 1V35 are NOT supported by the KRM-3Z7XXX modules as the I/O voltage is isolated by a high side P-FET switch which is only active after the modules power sub system reports power OK. Gate Voltages that do not at least reach 1V35 do not turn the P-FET on sufficiently; therefore 1V2 I/O voltages cannot be used reliably.



PL BANK X1_1

The PL Bank that is mapped to X1_1 is one of the two, fully featured I/O Banks. All 48 I/O's that are available on the KRM Module are accessible via FMC connector

PL BANK X1_1 Signal Table:

Module PIN	Signal Name	Destination PIN	Destination Name	Remark	I/O Level
X1_3	X1_1_000	FMC_H37	LA32_P		V ADJ 1V8 or 3V3
X1_5	X1_1_001	FMC_H38	LA32_N		V ADJ 1V8 or 3V3
X1_7	X1_1_002	FMC_G36	LA33_P		V ADJ 1V8 or 3V3
X1_9	X1_1_003	FMC_G37	LA33_N		V ADJ 1V8 or 3V3
X1_11	X1_1_004	FMC_H34	LA30_P		V ADJ 1V8 or 3V3
X1_13	X1_1_005	FMC_H35	LA30_N		V ADJ 1V8 or 3V3
X1_15	X1_1_006	FMC_G33	LA31_P		V ADJ 1V8 or 3V3
X1_17	X1_1_007	FMC_G34	LA31_N		V ADJ 1V8 or 3V3
X1_19	X1_1_008	FMC_H31	LA28_P		V ADJ 1V8 or 3V3
X1_21	X1_1_009	FMC_H32	LA28_N		V ADJ 1V8 or 3V3
X1_23	X1_1_010	FMC_G30	LA29_P		V ADJ 1V8 or 3V3
X1_25	X1_1_011	FMC_G31	LA29_N		V ADJ 1V8 or 3V3
X1_4	X1_1_100	FMC_H28	LA24_P		V ADJ 1V8 or 3V3
X1_6	X1_1_101	FMC_H29	LA24_N		V ADJ 1V8 or 3V3
X1_8	X1_1_102	FMC_G27	LA25_P		V ADJ 1V8 or 3V3
X1_10	X1_1_103	FMC_G28	LA25_N		V ADJ 1V8 or 3V3
X1_12	X1_1_104	FMC_C26	LA27_P		V ADJ 1V8 or 3V3
X1_14	X1_1_105	FMC_C27	LA27_N		V ADJ 1V8 or 3V3
X1_16	X1_1_106	FMC_D26	LA26_P		V ADJ 1V8 or 3V3
X1_18	X1_1_107	FMC_D27	LA26_N		V ADJ 1V8 or 3V3
X1_20	X1_1_108	FMC_G24	LA22_P	SRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_22	X1_1_109	FMC_G25	LA22_N	SRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_24	X1_1_110	FMC_D23	LA23_P	MRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_26	X1_1_111	FMC_D24	LA23_N	MRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_31	X1_1_200	FMC_H25	LA21_P	MRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_33	X1_1_201	FMC_H26	LA21_N	MRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_35	X1_1_202	FMC_H22	LA19_P	SRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_37	X1_1_203	FMC_H23	LA19_N	SRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_39	X1_1_204	FMC_G21	LA20_P		V ADJ 1V8 or 3V3
X1_41	X1_1_205	FMC_G22	LA20_N		V ADJ 1V8 or 3V3
X1_43	X1_1_206	FMC_C22	LA18_P_CC	NOT IDEAL CLOCK IN PIN ON FPGA	V ADJ 1V8 or 3V3
X1_45	X1_1_207	FMC_C23	LA18_N_CC	NOT IDEAL CLOCK IN PIN ON FPGA	V ADJ 1V8 or 3V3
X1_47	X1_1_208	FMC_D20	LA17_P_CC	NOT IDEAL CLOCK IN PIN ON FPGA	V ADJ 1V8 or 3V3
X1_49	X1_1_209	FMC_D21	LA17_N_CC	NOT IDEAL CLOCK IN PIN ON FPGA	V ADJ 1V8 or 3V3
X1_51	X1_1_210	FMC_G18	LA16_P		V ADJ 1V8 or 3V3
X1_53	X1_1_211	FMC_G19	LA16_N		V ADJ 1V8 or 3V3
X1_32	X1_1_300	FMC_H19	LA15_P		V ADJ 1V8 or 3V3
X1_34	X1_1_301	FMC_H20	LA15_N		V ADJ 1V8 or 3V3
X1_36	X1_1_302	FMC_C18	LA14_P		V ADJ 1V8 or 3V3
X1_38	X1_1_303	FMC_C19	LA14_N		V ADJ 1V8 or 3V3
X1_40	X1_1_304	FMC_D17	LA13_P		V ADJ 1V8 or 3V3
X1_42	X1_1_305	FMC_D18	LA13_N		V ADJ 1V8 or 3V3
X1_44	X1_1_306	FMC_H16	LA11_P		V ADJ 1V8 or 3V3
X1_46	X1_1_307	FMC_H17	LA11_N		V ADJ 1V8 or 3V3
X1_48	X1_1_308	FMC_G15	LA12_P		V ADJ 1V8 or 3V3
X1_50	X1_1_309	FMC_G16	LA12_N		V ADJ 1V8 or 3V3
X1_52	X1_1_310	FMC_C14	LA10_P		V ADJ 1V8 or 3V3
X1_54	X1_1_311	FMC_C15	LA10_N		V ADJ 1V8 or 3V3

PL BANK X1_2

The PL Bank that is mapped to X1_2 is one of the two, fully featured I/O Banks. The lower 24 I/Os that are available on the KRM Module are accessible via FMC connector. Selected signals of the upper 24 I/Os are available on PMOD compatible solder pads.

PL BANK X1_2 Signal Table:

Module PIN	Signal Name	Destination PIN	Destination Name	Remark	I/O Level
X1_57	X1_2_000	FMC_D14	LA09_P		V ADJ 1V8 or 3V3
X1_59	X1_2_001	FMC_D15	LA09_N		V ADJ 1V8 or 3V3
X1_61	X1_2_002	FMC_H13	LA07_P		V ADJ 1V8 or 3V3
X1_63	X1_2_003	FMC_H14	LA07_N		V ADJ 1V8 or 3V3
X1_65	X1_2_004	FMC_G12	LA08_P		V ADJ 1V8 or 3V3
X1_67	X1_2_005	FMC_G13	LA08_N		V ADJ 1V8 or 3V3
X1_69	X1_2_006	FMC_D11	LA05_P		V ADJ 1V8 or 3V3
X1_71	X1_2_007	FMC_D12	LA05_N		V ADJ 1V8 or 3V3
X1_73	X1_2_008	FMC_C10	LA06_P		V ADJ 1V8 or 3V3
X1_75	X1_2_009	FMC_C11	LA06_N		V ADJ 1V8 or 3V3
X1_77	X1_2_010	FMC_G2	CLK0_C2M_P		V ADJ 1V8 or 3V3
X1_79	X1_2_011	FMC_G3	CLK0_C2M_N		V ADJ 1V8 or 3V3
X1_58	X1_2_100	FMC_H10	LA04_P		V ADJ 1V8 or 3V3
X1_60	X1_2_101	FMC_H11	LA04_N		V ADJ 1V8 or 3V3
X1_62	X1_2_102	FMC_G9	LA03_P		V ADJ 1V8 or 3V3
X1_64	X1_2_103	FMC_G10	LA03_N		V ADJ 1V8 or 3V3
X1_66	X1_2_104	FMC_H7	LA02_P		V ADJ 1V8 or 3V3
X1_68	X1_2_105	FMC_H8	LA02_N		V ADJ 1V8 or 3V3
X1_70	X1_2_106	FMC_D8	LA01_P_CC	NOT IDEAL CLOCK IN PIN ON FPGA	V ADJ 1V8 or 3V3
X1_72	X1_2_107	FMC_D9	LA01_N_CC	NOT IDEAL CLOCK IN PIN ON FPGA	V ADJ 1V8 or 3V3
X1_74	X1_2_108	FMC_G6	LA00_P_CC	SRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_76	X1_2_109	FMC_G7	LA00_N_CC	SRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_78	X1_2_110	FMC_H4	CLK0_M2C_P	MRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_80	X1_2_111	FMC_H5	CLK0_M2C_N	MRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_85	X1_2_200	XP1_1		MRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_87	X1_2_201	XP1_2		MRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_89	X1_2_202	XP1_3		SRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_91	X1_2_203	XP1_4		SRCC PIN PAIR ON FPGA	V ADJ 1V8 or 3V3
X1_93	X1_2_204	XP2_1			V ADJ 1V8 or 3V3
X1_95	X1_2_205	XP2_2			V ADJ 1V8 or 3V3
X1_97	X1_2_206	XP2_3			V ADJ 1V8 or 3V3
X1_99	X1_2_207	XP2_4			V ADJ 1V8 or 3V3
X1_101	X1_2_208				V ADJ 1V8 or 3V3
X1_103	X1_2_209				V ADJ 1V8 or 3V3
X1_105	X1_2_210				V ADJ 1V8 or 3V3
X1_107	X1_2_211				V ADJ 1V8 or 3V3
X1_86	X1_2_300	XP3_1			V ADJ 1V8 or 3V3
X1_88	X1_2_301	XP3_2			V ADJ 1V8 or 3V3
X1_90	X1_2_302	XP3_3			V ADJ 1V8 or 3V3
X1_92	X1_2_303	XP3_4			V ADJ 1V8 or 3V3
X1_94	X1_2_304	XP4_1			V ADJ 1V8 or 3V3
X1_96	X1_2_305	XP4_2			V ADJ 1V8 or 3V3
X1_98	X1_2_306	XP4_3			V ADJ 1V8 or 3V3
X1_100	X1_2_307	XP4_4			V ADJ 1V8 or 3V3
X1_102	X1_2_308				V ADJ 1V8 or 3V3
X1_104	X1_2_309				V ADJ 1V8 or 3V3
X1_106	X1_2_310				V ADJ 1V8 or 3V3
X1_108	X1_2_311				V ADJ 1V8 or 3V3

FMC

The FMC connector's HPC section (high pin count) is partially populated with 8 MGT lanes (0 through7). Its LPC section (low pin count) is fully populated with LVDS or LVCMOS signals on columns C, D, G and H.
The polarity of the MGT differential pairs is swapped to facilitate an optimized layout. Use RX Polarity control settings as described in Table 4-28 of the Xilinx user guide UG476 to reverse the effect.

V-Adjust is driven by a dedicated 1A DC/DC converter which can be configured to supply voltages from 1V8 to 3V3. The same voltage is applied to the KRM I/O bank supply pins which connect to the LPC signals.

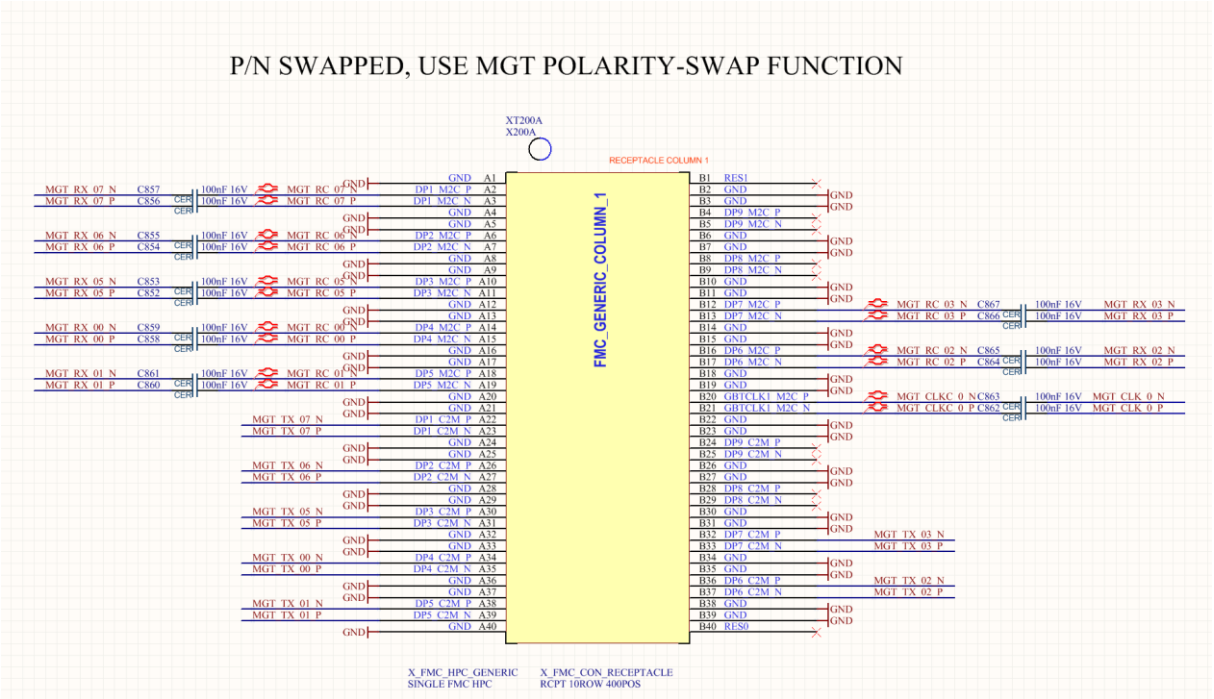
SCL and SDA are attached to the power manager and X2_1 306/7

JTAG signals can be daisy chained with the JTAG port of the SoM or bypass the SoM for direct connection to the JTAG connector. See quick start guide for details.

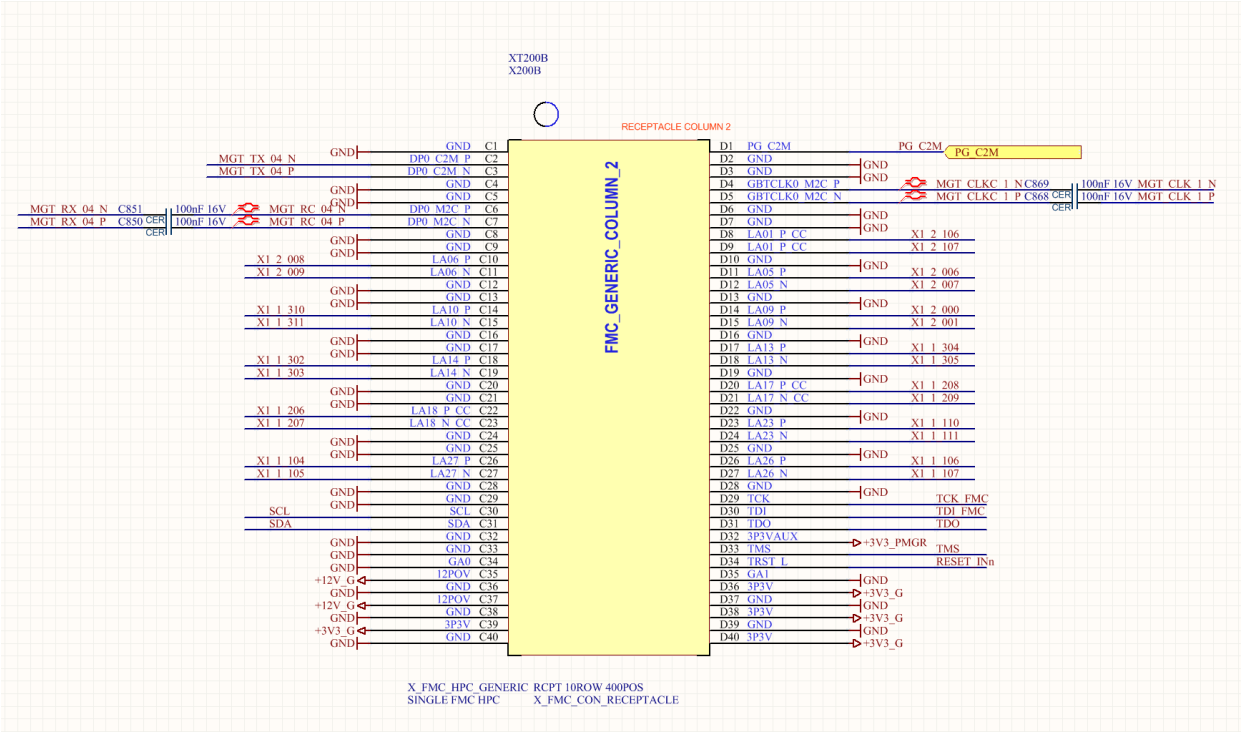
PG_C2M is driven by the power manager, indicating power good on the carrier.

PRSNT_M2C_L is monitored by the power manager. Currently the module presence detect has no function as the same bank also provides connectivity to the PMOD compatible connector field, therefore not all use cases justify the testing of an FMC module presence. This feature may be changed in a future release, please contact KR with any requests.

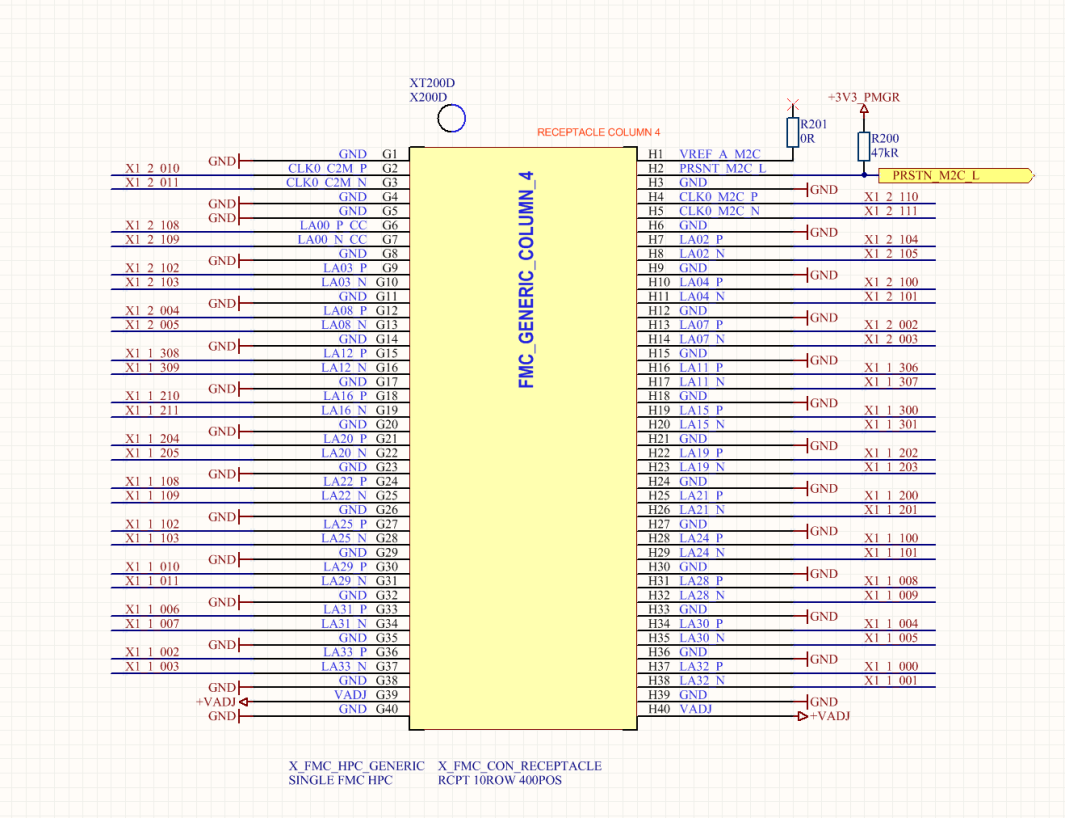
FMC Schematic of Column 1:



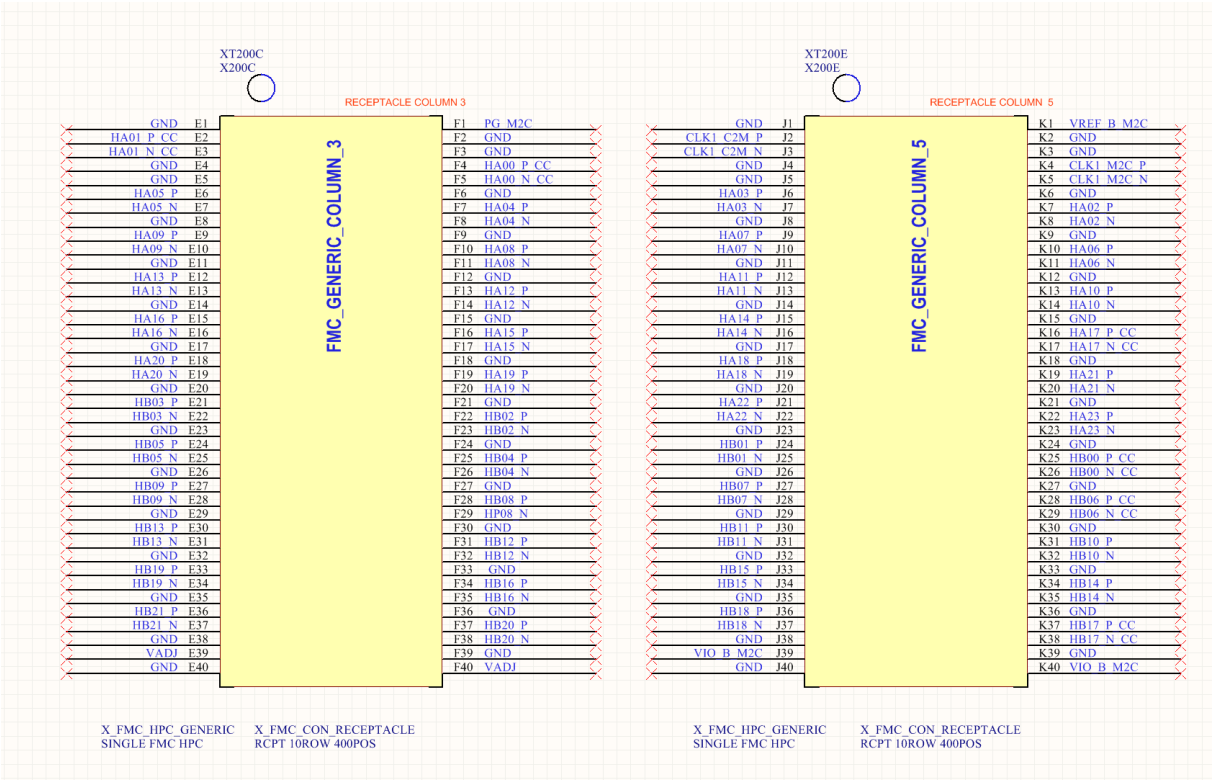
FMC Schematic of Column2:



FMC Schematic of Column 4:



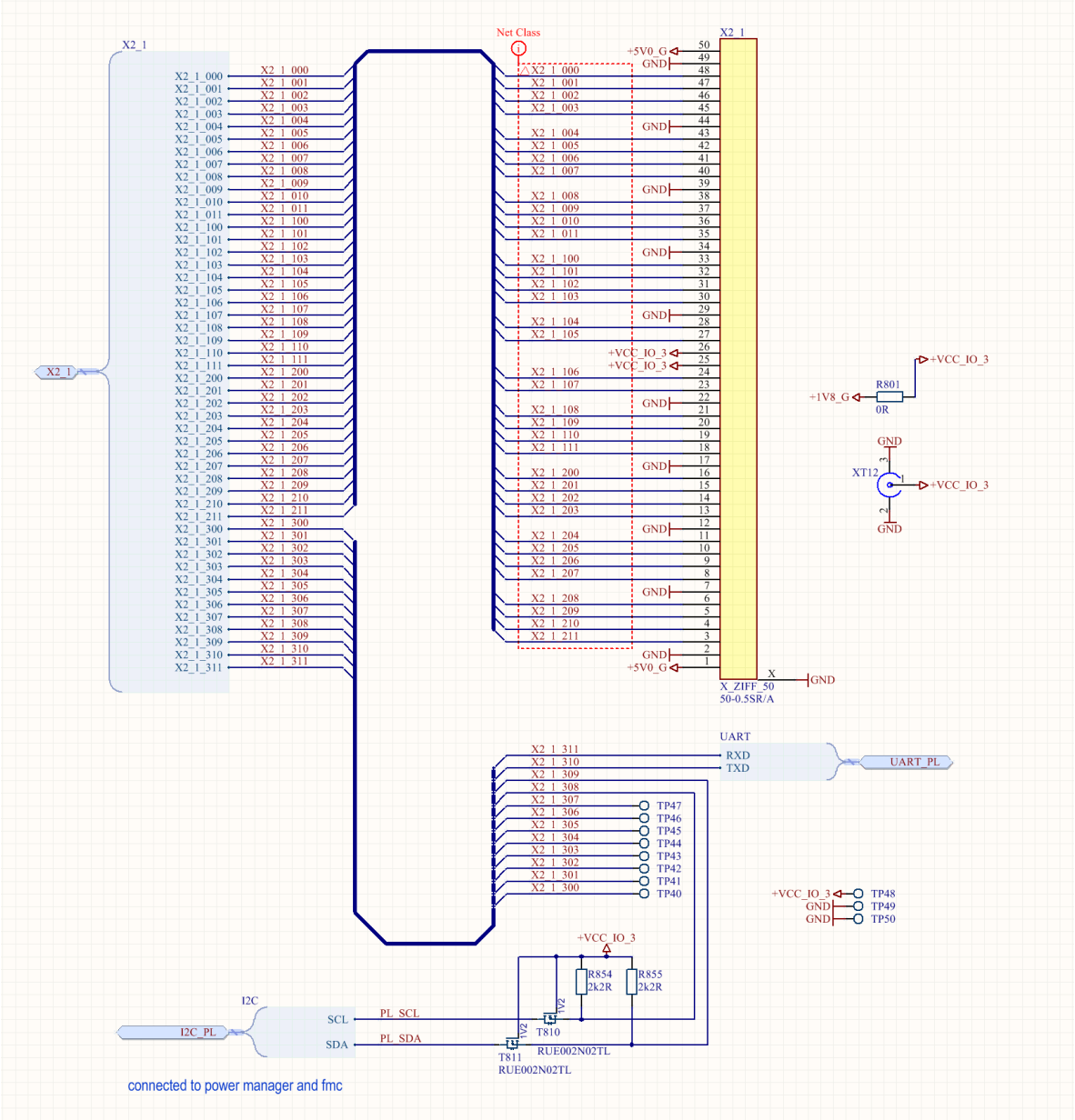
FMC Schematic of Columns 3&5:



PL BANK X2_1

The PL Bank that is mapped to X2_1 is one of the two general purpose PL I/O banks. Byte Lanes 0-2 are mapped to a 50 pin Ziff header which supports standard KR peripherals. Byte Lane 3 is connected to support a UART (optionally connected to the UART to USB Bridge) and an I2C port which is connected to the FMC connector & BMC via a level shifting circuit. The remaining pins are available on solder test points.
The orientation of the 50pin Ziff header facilitates the attachment of a touch display (for example the KRM-3500-DISPLAY)
The Bank's I/O Voltage is selected by populating R801 for 1V8 operation. If other operating voltages are desired, the resistor must be removed. The target supply voltage must be jumped to the open resistor pad with a wire. By default only the 1V8 Supply is an assembly option in order to ensure I/O Bank Voltage constraints are enforced for all of the KRM-3Z7xxx Modules. If a Module with Artix fabric is used, the supply may be jumped to Voltages up to 3V3. (KRM-3Z7020.. supports up to 3V3, KRM-3Z7030/035/045.. only support up to 1V8)

PL BANK X2_1 Schematic:

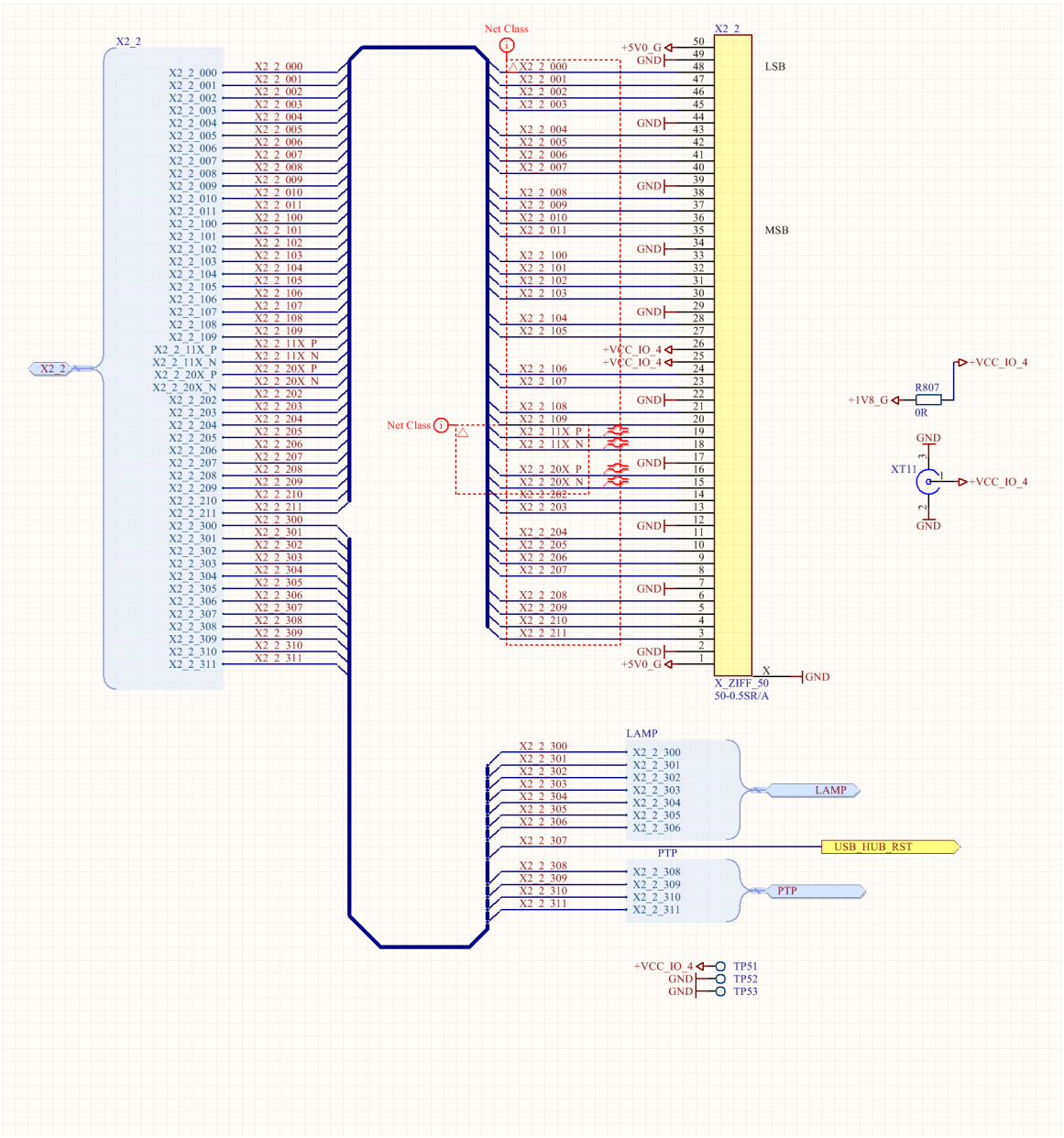


PL BANK X2_2

The PL Bank that is mapped to X2_2 is one of the two general purpose PL I/O banks. Byte Lanes 0-2 are mapped to a 50 pin ziff header which supports standard KR peripherals.
Byte Lane 3 is connected to drive user RGB LEDs and to optionally control the USB hub reset. If USB reset is not used by the host application, this signal should be driven to GND. Further signals are mapped to the Ethernet PHY's PTP signals via not populated resistors. This is a future option and currently not supported and may only be implemented if the bank operates on 1V8 I/O voltage.

The Bank's I/O Voltage is selected by populating R807 for 1V8 operation. If other operating voltages are desired, the resistor must be removed. The target supply voltage must be jumped to the open resistor pad with a wire. By default only the 1V8 Supply is an assembly option in order to ensure I/O Bank Voltage constraints are enforced for all of the KRM-3Z7xxx Modules. If a Module with Artix fabric is used, the supply may be jumped to Voltages up to 3V3. (KRM-3Z7020.. supports up to 3V3, KRM-3Z7030/035/045.. only support up to 1V8)

PL BANK X2_2 Schematic:



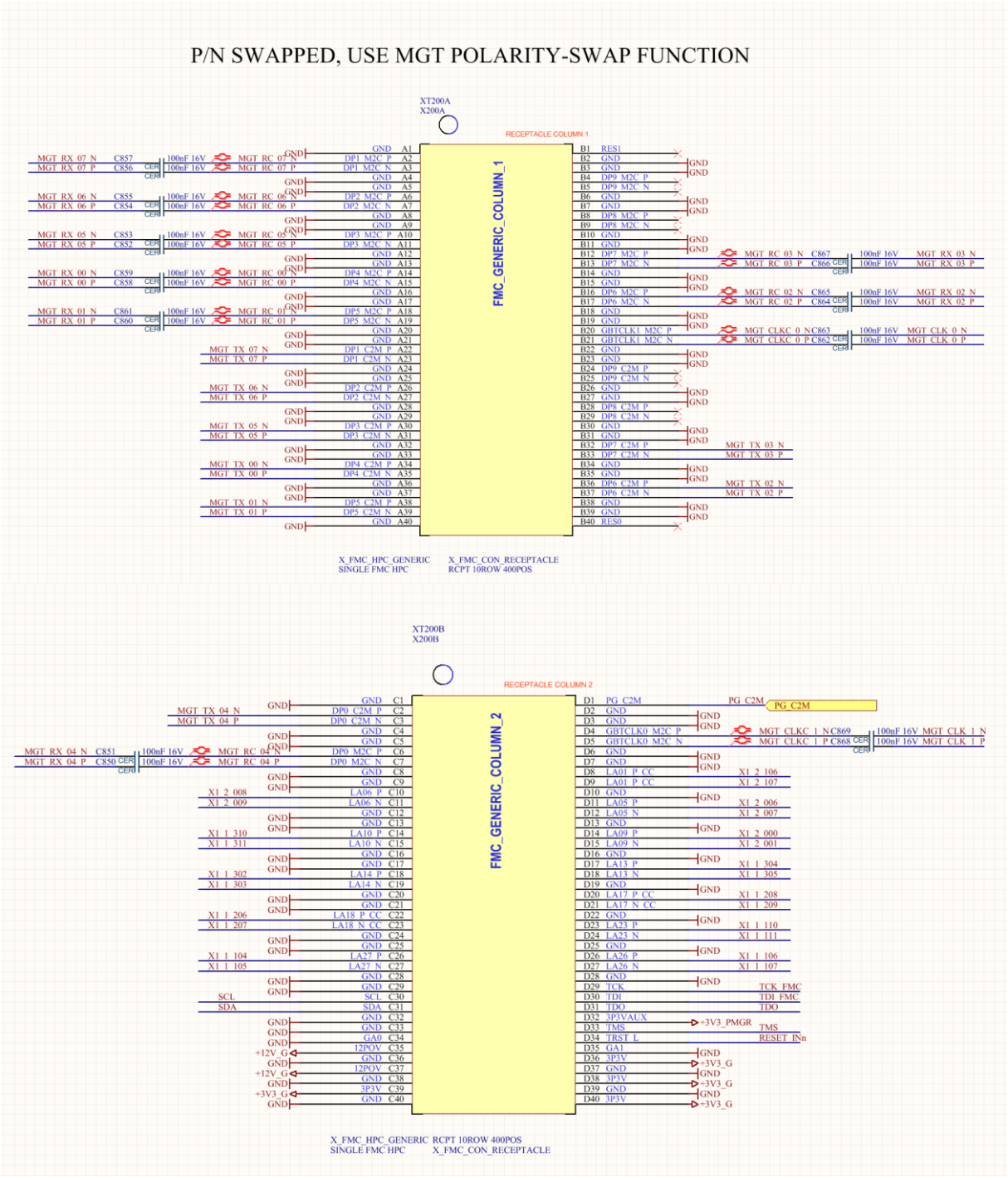
MGT IO

The KRC3701 carrier connects all eight MGT lanes and both reference clock pairs of the KRM-3Z7xxx module to the FMC connector.

MGT Signal Table:

Module PIN	Signal Name	Destination PIN	Destination Name	Remark
X1_111	X1_MGT_TX_00_P	FMC_A34	DP4_C2M_P	KRM-3Z7035/45 SUPPORT
X1_113	X1_MGT_TX_00_N	FMC_A35	DP4_C2M_N	
X1_117	X1_MGT_TX_01_P	FMC_A38	DP5_C2M_P	KRM-3Z7035/45 SUPPORT
X1_119	X1_MGT_TX_01_N	FMC_A39	DP5_C2M_N	
X1_123	X1_MGT_TX_02_P	FMC_B36	DP6_C2M_P	KRM-3Z7035/45 SUPPORT
X1_125	X1_MGT_TX_02_N	FMC_B37	DP6_C2M_N	
X1_129	X1_MGT_TX_03_P	FMC_B32	DP7_C2M_P	KRM-3Z7035/45 SUPPORT
X1_131	X1_MGT_TX_03_N	FMC_B33	DP7_C2M_N	
X1_141	X1_MGT_TX_04_P	FMC_C2	DP0_C2M_P	KRM-3Z7030/35/45 SUPPORT
X1_143	X1_MGT_TX_04_N	FMC_C3	DP0_C2M_N	
X1_147	X1_MGT_TX_05_P	FMC_A30	DP3_C2M_P	KRM-3Z7030/35/45 SUPPORT
X1_149	X1_MGT_TX_05_N	FMC_A31	DP3_C2M_N	
X1_153	X1_MGT_TX_06_P	FMC_A26	DP2_C2M_P	KRM-3Z7030/35/45 SUPPORT
X1_155	X1_MGT_TX_06_N	FMC_A27	DP2_C2M_N	
X1_159	X1_MGT_TX_07_P	FMC_A22	DP1_C2M_P	KRM-3Z7030/35/45 SUPPORT
X1_161	X1_MGT_TX_07_N	FMC_A23	DP1_C2M_N	
X1_112	X1_MGT_RX_00_P	FMC_A14	DP4_M2C_P	KRM-3Z7035/45 SUPPORT
X1_114	X1_MGT_RX_00_N	FMC_A15	DP4_M2C_N	
X1_118	X1_MGT_RX_01_P	FMC_A18	DP5_M2C_P	KRM-3Z7035/45 SUPPORT
X1_120	X1_MGT_RX_01_N	FMC_A19	DP5_M2C_N	
X1_124	X1_MGT_RX_02_P	FMC_B16	DP6_M2C_P	KRM-3Z7035/45 SUPPORT
X1_126	X1_MGT_RX_02_N	FMC_B17	DP6_M2C_N	
X1_130	X1_MGT_RX_03_P	FMC_B12	DP7_M2C_P	KRM-3Z7035/45 SUPPORT
X1_132	X1_MGT_RX_03_N	FMC_B13	DP7_M2C_N	
X1_142	X1_MGT_RX_04_P	FMC_C6	DP0_M2C_P	KRM-3Z7030/35/45 SUPPORT
X1_144	X1_MGT_RX_04_N	FMC_C7	DP0_M2C_N	
X1_148	X1_MGT_RX_05_P	FMC_A10	DP3_M2C_P	KRM-3Z7030/35/45 SUPPORT
X1_150	X1_MGT_RX_05_N	FMC_A11	DP3_M2C_N	
X1_154	X1_MGT_RX_06_P	FMC_A6	DP2_M2C_P	KRM-3Z7030/35/45 SUPPORT
X1_156	X1_MGT_RX_06_N	FMC_A7	DP2_M2C_N	
X1_160	X1_MGT_RX_07_P	FMC_A2	DP1_M2C_P	KRM-3Z7030/35/45 SUPPORT
X1_162	X1_MGT_RX_07_N	FMC_A3	DP1_M2C_N	
X1_135	X1_MGT_CLK_0_P	FMC_D4	GBTCLKC_1_M2C_P	KRM-3Z7035/45 SUPPORT
X1_137	X1_MGT_CLK_0_N	FMC_D5	GBTCLKC_1_M2C_N	
X1_136	X1_MGT_CLK_1_P	FMC_B20	GBTCLKC_0_M2C_P	KRM-3Z7030/35/45 SUPPORT
X1_138	X1_MGT_CLK_1_N	FMC_D21	GBTCLKC_0_M2C_N	

FMC MGT Schematic:



Thermal specification

Standard version:	Commercial operating range, 0°C to 70°C.
Industrial version:	Not available

Errata

HW Rev A:

No known errata.