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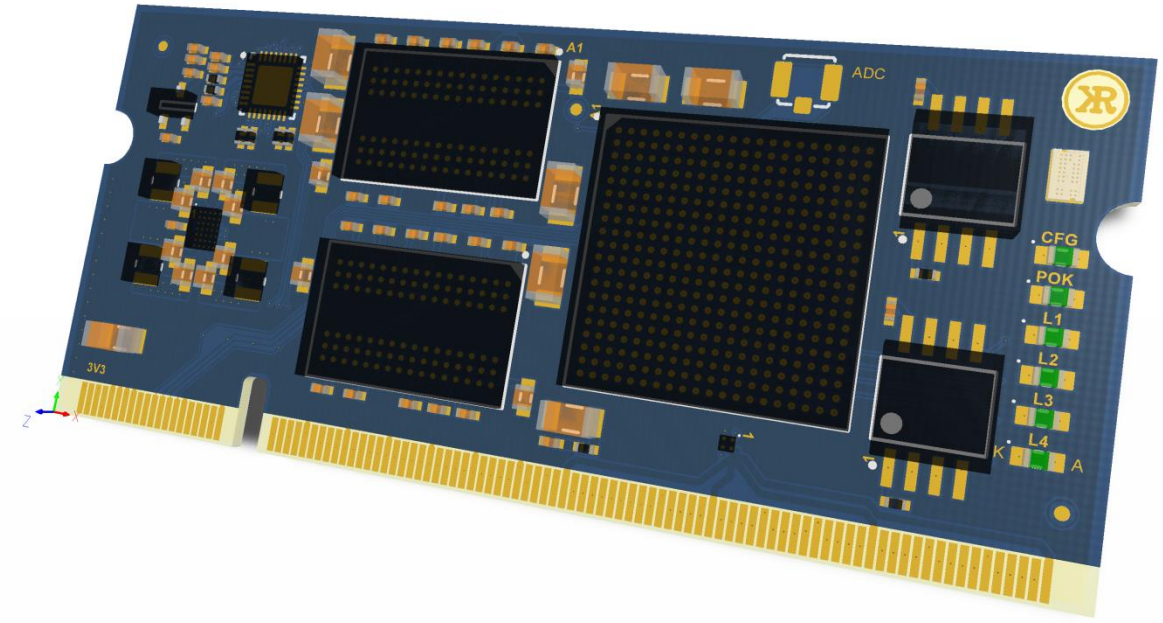
Switzerland GmbH

KRM-1Z70xx

Data sheet



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Revision History

Date	Document revision	HW revision	Changes
June 8th 2015	0.9	REV A	Initial document
October 12th 2015	1.0	REV A	First complete document for release
Jan 17th	1.1	REV A	Corrected naming to be in line with other families
Oct 27th	1.2	REV_B	First issue of REV B HW
November 7th 2019	1.3	REV_B	Updated Company address Refactoring Mode Pins part
Nov 30th 2019	1.4	REV_B	Normalized disclaimer with other KR datasheets Added recommended operating conditions Added absolute maximum ratings Added compliance section

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Assumptions

The reader is familiar with Xilinx FPGA and SoC components and the related terminology in common use.

Acronyms

FOM:	FPGA on Module
FU:	Future Use
KR:	Knowledge Resources GmbH
MIG:	Memory Interface Generator, a tool of Xilinx to easily implement a DDR3 controller
NA:	Not Applicable
PL:	Programmable Logic
PS:	Processing Subsystem
SoC:	System on Chip

Reference documents

ZYNQ all programmable SoC, Xilinx, www.xilinx.com

Support

KR will provide free of charge to qualified customers:

-Schematic and PCB libraries with Module and carrier board design components (Altium)
-3D STEP models of the module and heat spreader plate
-LINUX BSP and LINUX port (Plug and Boot ready)
-Reference schematics of the evaluation boards (Altium native and PDF)
-Vivado Project scripts to accelerate design starts

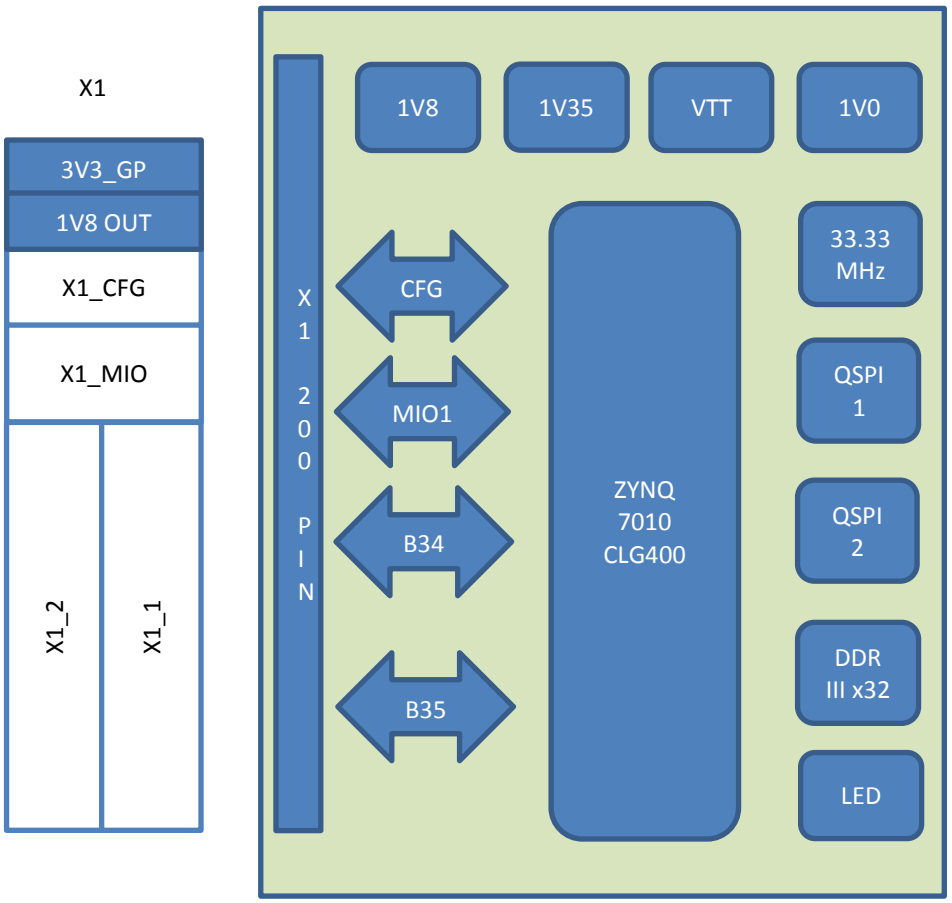
Further support to aid in customer specific design-in is available at competitive rates, please contact KR for details: + 41 61 545 2080 or mail to office@knowres.com

Introduction

With the KRM-1Z70XX, KR provides a highly flexible and cost-efficient board for FPGA and embedded systems prototyping. Due to its low cost, the KRM-1Z70XX is also suitable for integration in low to mid volume end-products. It is based on a Xilinx Zynq XC7Z010-1CLG400C SoC. The Xilinx SoC is accompanied by a 32 bit wide DDR3 memory subsystem on the PS, two instances of Quad SPI memory, power regulation, clock sources and 4 user LEDs.

The module's form-factor Corresponds to a standard SO-DIMM memory module and can be mated with a wide variety of SO-DIMM sockets.

Block diagram



Board dimensions

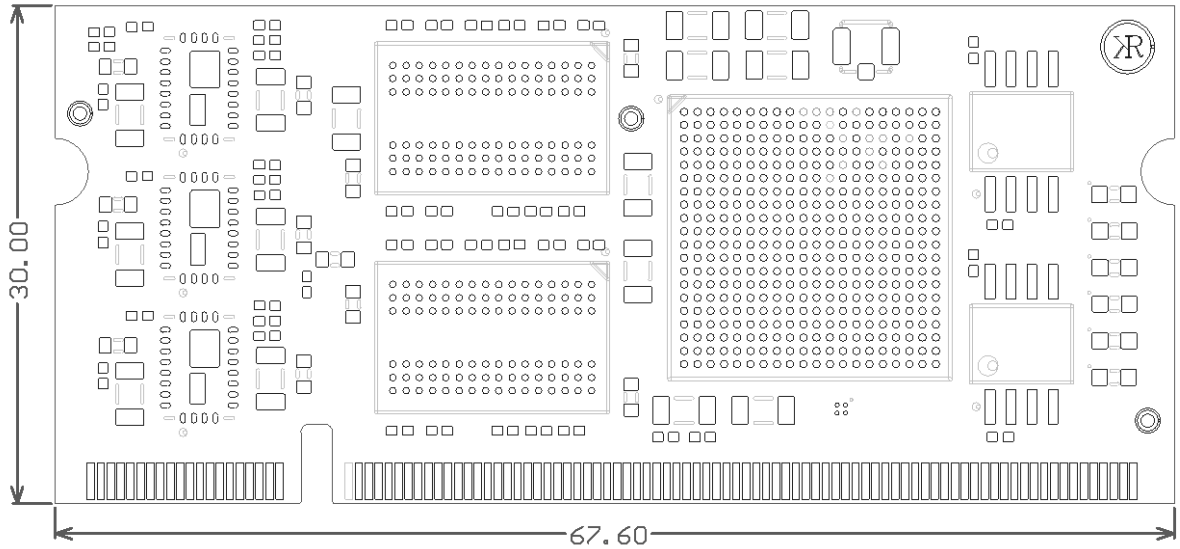


Figure 1: Board dimensions (in mm)

- Step models of the module are available
- Altium PCB and schematic templates are available

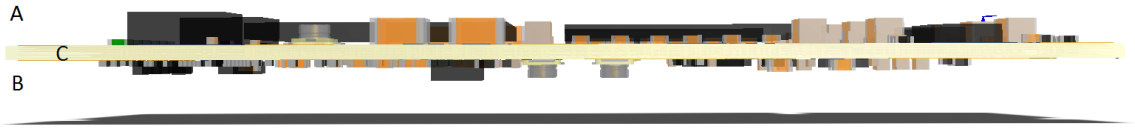


Figure 2: Board height

- A = Components max height top side 2.5mm +/- 0.1
- B = Components max height bottom side 1.8mm +/- 0.1
- C = PCB thickness 1mm +/- 0.1

Features

Overview

- Xilinx XC7Z010-1CLG400C
  - Available in speed grades 1 through 3; Commercial or industrial temperature range as options
  - 28K Logic Cells: 17’600 LUTs and 35’200 Flip-Flops
  - 80 DSP Slices /18x25 MACCs
  - 60 x 36Kb block RAMs, a total of 240 KB block RAM
  - Dual ARM A9 Cores with NEON co-processor
  - 256kB OC-RAM

- 8Gb LPDDR3 SDRAM PS memory

- 256Mbit QUAD SPI; 2 times 128Mbit

- 1X 200 pin SO-DIMMM I/O connectivity
  - 2x PL I/O bank (Banks 34, 35)
    - 48 pins each
    - All byte groups (0-3) intact and length matched
    - I/O voltage supplied by carrier board, can be different for each bank
    - External I/O Voltage is switched; switch is enabled by the on-board FPGA config done signal
  - 1x PS MIO1 bank
    - MIO 16 through 53 (all of bank 501)
    - 1V8 default, supplied by KRM on-board regulator
  - JTAG chain to FPGA; 3V3
  - PS reset in pin
  - CFG INn pin to initiate configuration process
  - Configuration OKn ; buffered open collector output
  - Power OKn out; open collector output

- Requires 3V3 supply
- Provides 1V8 up to 1.5A supply for peripherals on carrier board

- 33.333 MHz on-board oscillator

- 4 User LED driven by bank 34 & 35 I/O_0 and I/O_25 (not part of byte groups on I/O connector)

Power supply and power considerations

Core power

-The KRM-1Z70XX requires a **stable** power supply of 3V3. In order to support designs with high FPGA utilization, a supply capable of providing at least 1.5A is required, 3A is recommended.
-The 3V3 Global supply must be bypassed with a minimum of 47uF on the carrier board.
-Each Bank I/O supply pin must be bypassed with a minimum of 10uF on the carrier board.

I/O Bank Power sequence

I/O Bank power is to be supplied by the user design on the carrier board and may range from 1V35 to 3V3. The module generated 1V8 may be used to power carrier board peripherals
Each I/O bank may be powered by a different I/O voltage, for maximum flexibility of the module.
In order to ensure optimal power sequencing of the power rails as recommended by Xilinx, the I/O Bank power is switched by on-board FET so that the user does not have to be concerned about the power sequencing of I/O voltages. The power-up of the I/O banks is enabled by the "POK" of the on board regulators.

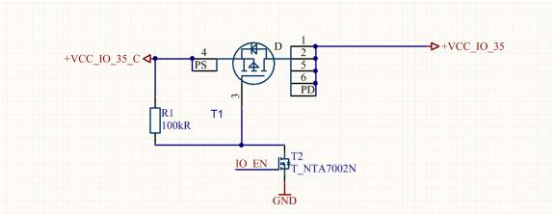


Figure 3

Supply Type	SO-DIMM pin number	Voltage	Current	Remark
Global Module supply for internal regulators and CFG circuits	X1: 1,2,3,4,5,6,7,8	3V3 Global	4.0A [i]	Bypass with at least 47uF on carrier
I/O Supply X1 GROUP1 (BANK 35)	X1: 110,140,170,200	1V35 to 3V3	600mA	Bypass with at least 4x 10uF on carrier
I/O Supply X1 GROUP2 (BANK 34)	X1: 109,139,169,199	1V35 to 3V3	600mA	Bypass with at least 4x 10uF on carrier

[i] The pin limited maximum power to the Module is 8x 0.5A @3.3V = 13.2W. Realistically power consumption is below 3W

Clocking resources

Onboard oscillator

The onboard oscillator provides 33.33 MHz to the PS PLL of the SoC.

External PL Fabric clocks

Each bank exposes all clock capable pins, please consult the KRM-1Z7010 I/O tables and Xilinx clocking guide for details.

Reset

-The PS reset port is available in the configuration and housekeeping signal group on connector X1: Pin22
-The reset pin is internally pulled up to 3V3 Global and forwarded to the PS reset pin via the BMC.
-The PS is internally held in reset until all onboard power supplies report power good.
-Power-on-reset is provided by the modules circuit; External reset is recommended but optional

Signal name	Board connector	Direction	Remark	I/O Level
RESET_INn	X1: 22	EDGE →FPGA	active low	INT PU to 3V3

Ready

-The module reports the conclusion of the configuration process via the signal CFG_OKn on connector X1:Pin28
-CFG_OKn is connected to a dedicated FET and implemented as an open drain output. It may sink as much as 50mA, an external pull-up resistor is required.
-CFG_OKn is driven by the Done_0 signal of the Zynq

Signal name	Board connector	Direction	Remark	I/O Level
CFG_OKn	X1: 28	FPGA→ EDGE	active low	OC

Configuration

JTAG Interface

The FPGA configuration file - i.e. the FPGA firmware - can be loaded via dedicated JTAG pins

	Signal name	Board connector	Direction	Remark	I/O Level
JTAG	TMS	X1:27	EDGE → FPGA	Pull to GND with 4k7R on carrier	3V3
	TCK	X1:25	EDGE → FPGA		3V3
	TDO	X1:23	FPGA → EDGE		3V3
	TDI	X1:21	EDGE → FPGA		3V3

Mode Pins

The MIO_0 Bank of the PS system (Bank 500) is dedicated to the modules internal functions such as configuration and housekeeping.

The mode pins are controlled by the BMC. Two pins of the BMC are accessible via the connector to alter the boot mode and the boot source.
When the connector PIN_31 (SD_QSPI) is low, the boot source is (external) SD. For example the card detect signal of an SD card holder may be used to toggle the configuration from QSPI to SD only when an SD card is inserted.

When the connector PIN_33 (SELF_JTAG) is low, the boot mode is set to JTAG even if the flash image is corrupted. (This is a recovery method if a faulty boot image was loaded to SPI, which may cause the Zynq to lock-up and not be reachable even by JTAG)

Mode pins MIO_02 through MIO_08 are largely dual-use; they determine the power-up-mode and are also used to implement the two QSPI interfaces.

On-Board Quad SPI Configuration Memory

Two instances of QSPI memory are implemented on the module.

Each instance is populated with a 128Mbit QSPI flash.

	Signal name	MIO	Direction	Remark	I/O Level
QSPI0	S#	MIO_01	FPGA → SPI	Pull up on Module	3V3
	DQ0	MIO_02	BI-DIR		3V3
	DQ1	MIO_03	BI-DIR		3V3
	DQ2/W#	MIO_04	BI-DIR		3V3
	DQ3/HOLD#	MIO_05	BI-DIR		3V3
	CLK	MIO_06	FPGA → SPI		3V3

	Signal name	MIO	Direction	Remark	I/O Level
QSPI1	S#	MIO_00	FPGA → SPI	Pull up on Module	3V3
	DQ0	MIO_10	BI-DIR		3V3
	DQ1	MIO_11	BI-DIR		3V3
	DQ2/W#	MIO_12	BI-DIR		3V3
	DQ3/HOLD#	MIO_13	BI-DIR		3V3
	CLK	MIO_09	FPGA → SPI		3V3

DDR3 SDRAM

-The KRM-1Z70XX PS memory is populated with DDR3 SDRAM providing a total of 8Gb of RAM, organized as 256M x 32 bit (1GB).
-The Memory subsystem can run as fast as 1066MT/s even on the slowest speed grade SoC.
-The KRM-1Z70XX implementation takes advantage of the lower power requirements of 1.35V operation.

I/O Connectivity

	Group	FPGA Bank	Remark	I/O Level
X1	X1_1	Bank 35	3V3 MAX high range	3V3 to 1V35
	X1_2	Bank 34	3V3 MAX high range	3V3 to 1V35
	X1_CFG	CFG		3V3
	X1_MIO	MIO_1/501	1V8	1V8

PL BANKS

- The Byte-groups of a PL I/O bank (T0 –T3) are kept as a group and are length matched on the module.
- Differential I/O capable pins of the PL are routed as coupled differential pairs.
- The uppermost and lowermost pin of each I/O Bank is not routed to the module edge connector but used to drive 4 user LED on the module.

MIO BANK

The MIO Bank I/O voltage is 1V8. MIO signals 16 through 53 (Bank 501) are available. In order to be compatible with KR issued Linux BSP's we recommend using the MIO assignment as shown on the Connector schematic. Naturally other configurations are possible, contact KR for BSP support of your desired configuration.

Connector Schematic

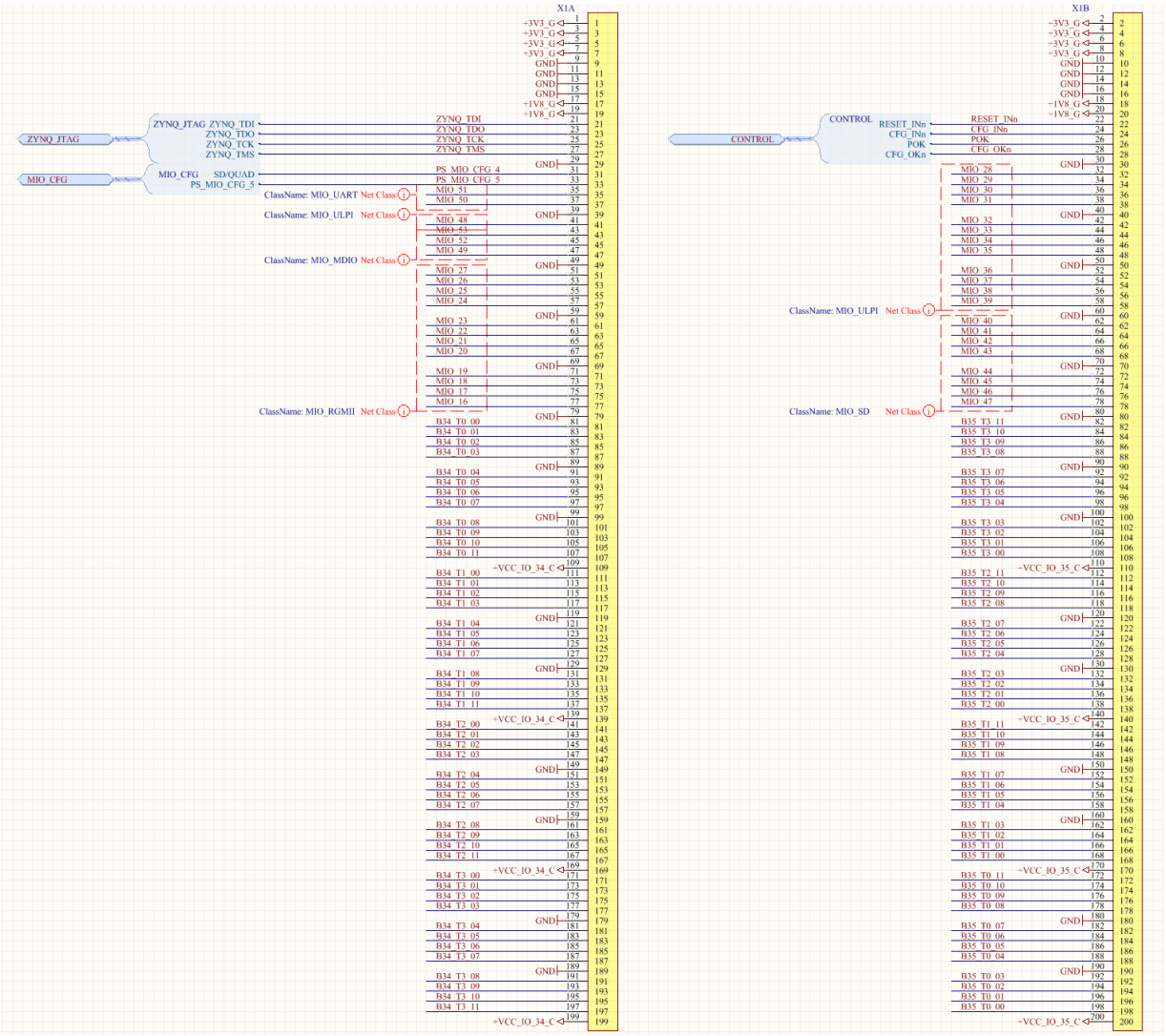


Figure 4: Connector signal assignments

Pin Mapping

Module Function	Module Pin	FPGA Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
CFG	NA	PS_MIO0_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_S#
CFG	NA	PS_MIO1_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_S#
CFG	NA	PS_MIO9_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_CLK
CFG	NA	PS_MIO10_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_DQ0
CFG	NA	PS_MIO11_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_DQ1
CFG	NA	PS_MIO12_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_DQ2
CFG	NA	PS_MIO13_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_DQ3
CFG_MODE	NA	PS_MIO2_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_DQ0
CFG_MODE	NA	PS_MIO3_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_DQ1
CFG_MODE	NA	PS_MIO6_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_CLK
CFG_MODE	NA	PS_MIO7_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	MODE_PIN
CFG_MODE	NA	PS_MIO8_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	MODE_PIN
CLK_IN	NA	PS_CLK_500	NA	500	MIO	OB_INT	+3V3_GLOBAL	33MHZ
LED_1	NA	IO_25_35	NA	35	HR	OB_LED	VIO_X1_1	USR_LED_1
LED_2	NA	IO_0_35	NA	35	HR	OB_LED	VIO_X1_1	USR_LED_2
LED_3	NA	IO_25_34	NA	34	HR	OB_LED	VIO_X1_2	USR_LED_3
LED_4	NA	IO_0_34	NA	34	HR	OB_LED	VIO_X1_2	USR_LED_4
POWER_IN	**X1:001**	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:002**	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:003**	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:004**	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:005**	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:006**	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:007**	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:008**	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
GND	**X1:009**	GND	NA	NA	NA	GLOBAL	GND	
GND	**X1:010**	GND	NA	NA	NA	GLOBAL	GND	
GND	**X1:011**	GND	NA	NA	NA	GLOBAL	GND	
GND	**X1:012**	GND	NA	NA	NA	GLOBAL	GND	
GND	**X1:013**	GND	NA	NA	NA	GLOBAL	GND	
GND	**X1:014**	GND	NA	NA	NA	GLOBAL	GND	
GND	**X1:015**	GND	NA	NA	NA	GLOBAL	GND	
GND	**X1:016**	GND	NA	NA	NA	GLOBAL	GND	
POWER_OUT	**X1:017**	1V8_G	NA	NA	NA		1V8 REG	OUTPUT !
POWER_OUT	**X1:018**	1V8_G	NA	NA	NA		1V8 REG	OUTPUT !
POWER_OUT	**X1:019**	1V8_G	NA	NA	NA		1V8 REG	OUTPUT !
POWER_OUT	**X1:020**	1V8_G	NA	NA	NA		1V8 REG	OUTPUT !
JTAG	**X1:021**	TDI_0	NA	0	CONFIG	X1_CFG	+3V3_GLOBAL	
PS_RST	**X1:022**	PS_SRST_B_501	NA	501	MIO	X1_MIO	Int PU	Ext OC/OD
JTAG	**X1:023**	TDO_0	NA	0	CONFIG	X1_CFG	+3V3_GLOBAL	

Module Function	Module Pin	FPGA Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
CFG_INn	**X1:024**	PS_POR_B_501	NA	0	CONFIG	X1_CFG	+3V3_GLOBAL	Int buffer
JTAG	**X1:025**	TCK_0	NA	0	CONFIG	X1_CFG	+3V3_GLOBAL	
POK	**X1:026**	POK	NA	NA	PWR		+3V3_GLOBAL	Int PU to 3V3
JTAG	**X1:027**	TMS_0	NA	0	CONFIG	X1_CFG	+3V3_GLOBAL	
CFG_OK	**X1:028**	DONE_0	NA	0	CONFIG	X1_CFG	VCC_0_MIO0	CFG_OKn open drain
GND	**X1:029**	GND	NA	NA	NA	X1_CFG	GND	CFG
GND	**X1:030**	GND	NA	NA	NA	X1_CFG	GND	CFG
CFG_MODE	**X1:031**	PS_MIO4_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_DQ2
PS_IO	**X1:032**	PS_MIO28_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
CFG_MODE	**X1:033**	PS_MIO5_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_DQ3
PS_IO	**X1:034**	PS_MIO29_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:035**	PS_MIO51_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:036**	PS_MIO30_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:037**	PS_MIO50_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:038**	PS_MIO31_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
GND	**X1:039**	GND	NA	NA	NA	X1_MIO	GND	MIO
GND	**X1:040**	GND	NA	NA	NA	X1_MIO	GND	MIO
PS_IO	**X1:041**	PS_MIO48_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:042**	PS_MIO32_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:043**	PS_MIO53_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:044**	PS_MIO33_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:045**	PS_MIO52_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:046**	PS_MIO34_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:047**	PS_MIO49_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:048**	PS_MIO35_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
GND	**X1:049**	GND	NA	NA	NA	X1_MIO	GND	MIO
GND	**X1:050**	GND	NA	NA	NA	X1_MIO	GND	MIO
PS_IO	**X1:051**	PS_MIO27_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:052**	PS_MIO36_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:053**	PS_MIO26_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:054**	PS_MIO37_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:055**	PS_MIO25_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:056**	PS_MIO38_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:057**	PS_MIO24_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:058**	PS_MIO39_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
GND	**X1:059**	GND	NA	NA	NA	X1_MIO	GND	MIO
GND	**X1:060**	GND	NA	NA	NA	X1_MIO	GND	MIO
PS_IO	**X1:061**	PS_MIO23_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:062**	PS_MIO40_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:063**	PS_MIO22_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:064**	PS_MIO41_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8

Module Function	Module Pin	FPGA Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PS_IO	**X1:065**	PS_MIO21_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:066**	PS_MIO42_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:067**	PS_MIO20_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:068**	PS_MIO43_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
GND	**X1:069**	GND	NA	NA	NA	X1_MIO	GND	MIO
GND	**X1:070**	GND	NA	NA	NA	X1_MIO	GND	MIO
PS_IO	**X1:071**	PS_MIO19_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:072**	PS_MIO44_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:073**	PS_MIO18_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:074**	PS_MIO45_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:075**	PS_MIO17_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:076**	PS_MIO46_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:077**	PS_MIO16_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
PS_IO	**X1:078**	PS_MIO47_501	NA	501	MIO	X1_MIO	1V8_OB	+1V8
GND	**X1:079**	GND	NA	NA	NA	X1_2	GND	B34
GND	**X1:080**	GND	NA	NA	NA	X1_1	GND	B35
PL_IO	**X1:081**	IO_L1P_T0_34	0	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:082**	IO_L24N_T3_AD15N_35	3	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:083**	IO_L1N_T0_34	0	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:084**	IO_L24P_T3_AD15P_35	3	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:085**	IO_L2P_T0_34	0	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:086**	IO_L23N_T3_35	3	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:087**	IO_L2N_T0_34	0	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:088**	IO_L23P_T3_35	3	35	HR	X1_1	VIO_X1_1	
GND	**X1:089**	GND	NA	NA	NA	X1_2	GND	B34
GND	**X1:090**	GND	NA	NA	NA	X1_1	GND	B35
PL_IO	**X1:091**	IO_L3P_T0_DQS_PUDC_B_34	0	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:092**	IO_L22N_T3_AD7N_35	3	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:093**	IO_L3N_T0_DQS_34	0	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:094**	IO_L22P_T3_AD7P_35	3	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:095**	IO_L4P_T0_34	0	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:096**	IO_L21N_T3_DQS_AD14N_35	3	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:097**	IO_L4N_T0_34	0	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:098**	IO_L21P_T3_DQS_AD14P_35	3	35	HR	X1_1	VIO_X1_1	
GND	**X1:099**	GND	NA	NA	NA	X1_2	GND	B34
GND	**X1:100**	GND	NA	NA	NA	X1_1	GND	B35
PL_IO	**X1:101**	IO_L5P_T0_34	0	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:102**	IO_L20N_T3_AD6N_35	3	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:103**	IO_L5N_T0_34	0	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:104**	IO_L20P_T3_AD6P_35	3	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:105**	IO_L6P_T0_34	0	34	HR	X1_2	VIO_X1_2	

Module Function	Module Pin	FPGA Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	**X1:106**	IO_L19N_T3_VREF_35	3	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:107**	IO_L6N_T0_VREF_34	0	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:108**	IO_L19P_T3_35	3	35	HR	X1_1	VIO_X1_1	
VCCO_34	**X1:109**	VCCO_34	NA	34	HR	X1_2	VIO_X1_2	USER DEF
VCCO_35	**X1:110**	VCCO_35	NA	35	HR	X1_1	VIO_X1_1	USER DEF
PL_IO	**X1:111**	IO_L7P_T1_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:112**	IO_L18N_T2_AD13N_35	2	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:113**	IO_L7N_T1_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:114**	IO_L18P_T2_AD13P_35	2	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:115**	IO_L8P_T1_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:116**	IO_L17N_T2_AD5N_35	2	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:117**	IO_L8N_T1_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:118**	IO_L17P_T2_AD5P_35	2	35	HR	X1_1	VIO_X1_1	
GND	**X1:119**	GND	NA	NA	NA	X1_2	GND	B34
GND	**X1:120**	GND	NA	NA	NA	X1_1	GND	B35
PL_IO	**X1:121**	IO_L9P_T1_DQS_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:122**	IO_L16N_T2_35	2	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:123**	IO_L9N_T1_DQS_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:124**	IO_L16P_T2_35	2	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:125**	IO_L10P_T1_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:126**	IO_L15N_T2_DQS_AD12N_35	2	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:127**	IO_L10N_T1_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:128**	IO_L15P_T2_DQS_AD12P_35	2	35	HR	X1_1	VIO_X1_1	
GND	**X1:129**	GND	NA	NA	NA	X1_2	GND	B34
GND	**X1:130**	GND	NA	NA	NA	X1_1	GND	B35
PL_IO	**X1:131**	IO_L11P_T1_SRCC_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:132**	IO_L14N_T2_AD4N_SRCC_35	2	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:133**	IO_L11N_T1_SRCC_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:134**	IO_L14P_T2_AD4P_SRCC_35	2	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:135**	IO_L12P_T1_MRCC_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:136**	IO_L13N_T2_MRCC_35	2	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:137**	IO_L12N_T1_MRCC_34	1	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:138**	IO_L13P_T2_MRCC_35	2	35	HR	X1_1	VIO_X1_1	
VCCO_34	**X1:139**	VCCO_34	NA	34	HR	X1_2	VIO_X1_2	USER DEF
VCCO_35	**X1:140**	VCCO_35	NA	35	HR	X1_1	VIO_X1_1	USER DEF
PL_IO	**X1:141**	IO_L13P_T2_MRCC_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:142**	IO_L12N_T1_MRCC_35	1	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:143**	IO_L13N_T2_MRCC_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:144**	IO_L12P_T1_MRCC_35	1	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:145**	IO_L14P_T2_SRCC_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:146**	IO_L11N_T1_SRCC_35	1	35	HR	X1_1	VIO_X1_1	

Module Function	Module Pin	FPGA Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	**X1:147**	IO_L14N_T2_SRCC_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:148**	IO_L11P_T1_SRCC_35	1	35	HR	X1_1	VIO_X1_1	
GND	**X1:149**	GND	NA	NA	NA	X1_2	GND	B34
GND	**X1:150**	GND	NA	NA	NA	X1_1	GND	B35
PL_IO	**X1:151**	IO_L15P_T2_DQS_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:152**	IO_L10N_T1_AD11N_35	1	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:153**	IO_L15N_T2_DQS_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:154**	IO_L10P_T1_AD11P_35	1	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:155**	IO_L16P_T2_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:156**	IO_L9N_T1_DQS_AD3N_35	1	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:157**	IO_L16N_T2_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:158**	IO_L9P_T1_DQS_AD3P_35	1	35	HR	X1_1	VIO_X1_1	
GND	**X1:159**	GND	NA	NA	NA	X1_2	GND	B34
GND	**X1:160**	GND	NA	NA	NA	X1_1	GND	B35
PL_IO	**X1:161**	IO_L17P_T2_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:162**	IO_L8N_T1_AD10N_35	1	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:163**	IO_L17N_T2_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:164**	IO_L8P_T1_AD10P_35	1	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:165**	IO_L18P_T2_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:166**	IO_L7N_T1_AD2N_35	1	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:167**	IO_L18N_T2_34	2	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:168**	IO_L7P_T1_AD2P_35	1	35	HR	X1_1	VIO_X1_1	
VCCO_34	**X1:169**	VCCO_34	NA	34	HR	X1_2	VIO_X1_2	USER DEF
VCCO_35	**X1:170**	VCCO_35	NA	35	HR	X1_1	VIO_X1_1	USER DEF
PL_IO	**X1:171**	IO_L19P_T3_34	3	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:172**	IO_L6N_T0_VREF_35	0	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:173**	IO_L19N_T3_VREF_34	3	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:174**	IO_L6P_T0_35	0	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:175**	IO_L20P_T3_34	3	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:176**	IO_L5N_T0_AD9N_35	0	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:177**	IO_L20N_T3_34	3	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:178**	IO_L5P_T0_AD9P_35	0	35	HR	X1_1	VIO_X1_1	
GND	**X1:179**	GND	NA	NA	NA	X1_2	GND	B34
GND	**X1:180**	GND	NA	NA	NA	X1_1	GND	B35
PL_IO	**X1:181**	IO_L21P_T3_DQS_34	3	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:182**	IO_L4N_T0_35	0	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:183**	IO_L21N_T3_DQS_34	3	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:184**	IO_L4P_T0_35	0	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:185**	IO_L22P_T3_34	3	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:186**	IO_L3N_T0_DQS_AD1N_35	0	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:187**	IO_L22N_T3_34	3	34	HR	X1_2	VIO_X1_2	

Module Function	Module Pin	FPGA Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	**X1:188**	IO_L3P_T0_DQS_AD1P_35	0	35	HR	X1_1	VIO_X1_1	
GND	**X1:189**	GND	NA	NA	NA	X1_2	GND	B34
GND	**X1:190**	GND	NA	NA	NA	X1_1	GND	B35
PL_IO	**X1:191**	IO_L23P_T3_34	3	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:192**	IO_L2N_T0_AD8N_35	0	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:193**	IO_L23N_T3_34	3	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:194**	IO_L2P_T0_AD8P_35	0	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:195**	IO_L24P_T3_34	3	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:196**	IO_L1N_T0_AD0N_35	0	35	HR	X1_1	VIO_X1_1	
PL_IO	**X1:197**	IO_L24N_T3_34	3	34	HR	X1_2	VIO_X1_2	
PL_IO	**X1:198**	IO_L1P_T0_AD0P_35	0	35	HR	X1_1	VIO_X1_1	
VCCO_34	**X1:199**	VCCO_34	NA	34	HR	X1_2	VIO_X1_2	USER DEF
VCCO_35	**X1:200**	VCCO_35	NA	35	HR	X1_1	VIO_X1_1	USER DEF

Compliance

All KRM modules are ROHSII and REACH compliant. For further details, customers may request the current declaration of conformity by emailing office@knowres.ch.
All KRM Modules are manufactured with UL94V-0 flammability rated PCBs with an IPC Class2 quality rating.

Electrical Specification

ESD

KRM Modules are sensitive to electrostatic discharge and must be handled with proper ESD precautions.

Absolute Maximum Ratings[i]

Symbol	Description	Min	Max
POWER_IN	Global power in	-0V5	3V6
VCCO_34/35	HR Bank I/O power supply	-0V5	3V6
V_BATT_IN	Encryption key storage supply	-0V5	2V0
PS_IO	MIO Bank I/O signal levels	-0V5	2V0
PL_IO_HR	HR Bank I/O signal levels	-0V5	3V6

Recommended Operating conditions

Symbol	Description	Min	Typ	Max
POWER_IN	Global power in	3V2	3V3	3V4
VCCO_34/35	HP Bank I/O power supply	1V7	1V8	1V89
V_BATT_IN	Encryption key storage supply	1V0	--	1V89
PS_IO	MIO Bank I/O signal levels[ii]	-0V2	--	VCCO + 0V2
PL_IO_HR	HR Bank I/O signal levels	-0V2	--	VCCO + 0V2

[i] Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied.
Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect module reliability
[ii] For I/O operation, refer to the Xilinx *7 Series FPGAs SelectIO Resources User Guide* (UG471) or the Xilinx *Zynq-7000 SoC Technical Reference Manual* (UG585).

Thermal specification

Absolute Maximum Ratings[iii]

Symbol	Description	Min	Max
Delta T	Max temperature change per second while operating	--	+/-1°C/sec
TSTG	Storage temperature ambient un-powered	-40°C	+125°C

Recommended Operating Conditions

Symbol	Description	Min	Typ	Max
Tj C	Operating Junction temperature of FPGA for commercial grade	0°C	--	+70°C
Tj I	Operating Junction temperature of FPGA for industrial grade	-40°C	--	+85°C
Delta T	Allowed temperature change per second while operating	--	--	+/-0.5°C/sec

[iii] Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied.

Module configurations

The KRM1-Z7xxx Modules can be purchased in a multitude of configurations as shown in the table below. Option codes shown in black are valid options for this family, not all valid options may be combined (for example boot option set to on-board QSPI, but no Flash populated is invalid). Blue option codes may become future options of this module family or may apply to a different version.

Standard Low quantity configuration

The standard assembly variant, which is orderable as samples, is as follows:

KRM-Z7010C1XBAC-B

Which corresponds to SODIMM module family, with a Zynq 7010, commercial speed grade, standard power rating, 1GB PS RAM and dual QSPI (32MB total) populated and boot mode selectable via user pin.

Configuration table