KNOWLEDGE RESOURCES
Switzerland GmbH

KRM-3ZU02/03/04/05

Data sheet Rev 0.2Preliminary

Knowledge Resources GmbH
Ackerstrase 30
CH – 4057 Basel
Switzerland

www.knowres.com

Table of Contents

Revision History

Date	Document revision	HW revision	Changes
October 22th 2019	0.1	REV B	Initial document
November 30th 2019	0.2	REV D	Minor corrections Updated configuration option codes

Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of KR products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, KR hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) KR shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or KR had been advised of the possibility of the same. KR assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications.

KR's products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of KR's products in such critical applications.

Trademark Acknowledgement:
Brand and product names mentioned in the Materials are trademarks or registered trademarks of their respective owners.

Assumptions

The reader is familiar with Xilinx FPGA and SoC components and the related terminology in common use.

Acronyms

FOM: FPGA on Module
FU: Future Use
KR: Knowledge Resources GmbH
MIG: Memory Interface Generator, a tool of Xilinx to easily implement a DDR3 controller
NA: Not Applicable
PL: Programmable Logic
PS: Processing Subsystem
MPSoC: Multi Processor System on Chip
BMC: Board Management Controller

Reference documents

ZYNQ all programmable SoC, Xilinx, www.xilinx.com
DDR4 SDRAM, Micron, www.micron.com
QSPI Flash memory, Micron, www.micron.com

Support

KR will provide free of charge to qualified customers:

-Schematic and PCB libraries with Module and carrier board design components (Altium),
-3D STEP models of the module and heat spreader plate,
-LINUX BSP and LINUX port (Plug and Boot ready),
-Reference schematics of the evaluation boards (Altium native and PDF),
-Reference designs for on-board PL memory use,
-Project scripts for Vivado to accelerate design starts.

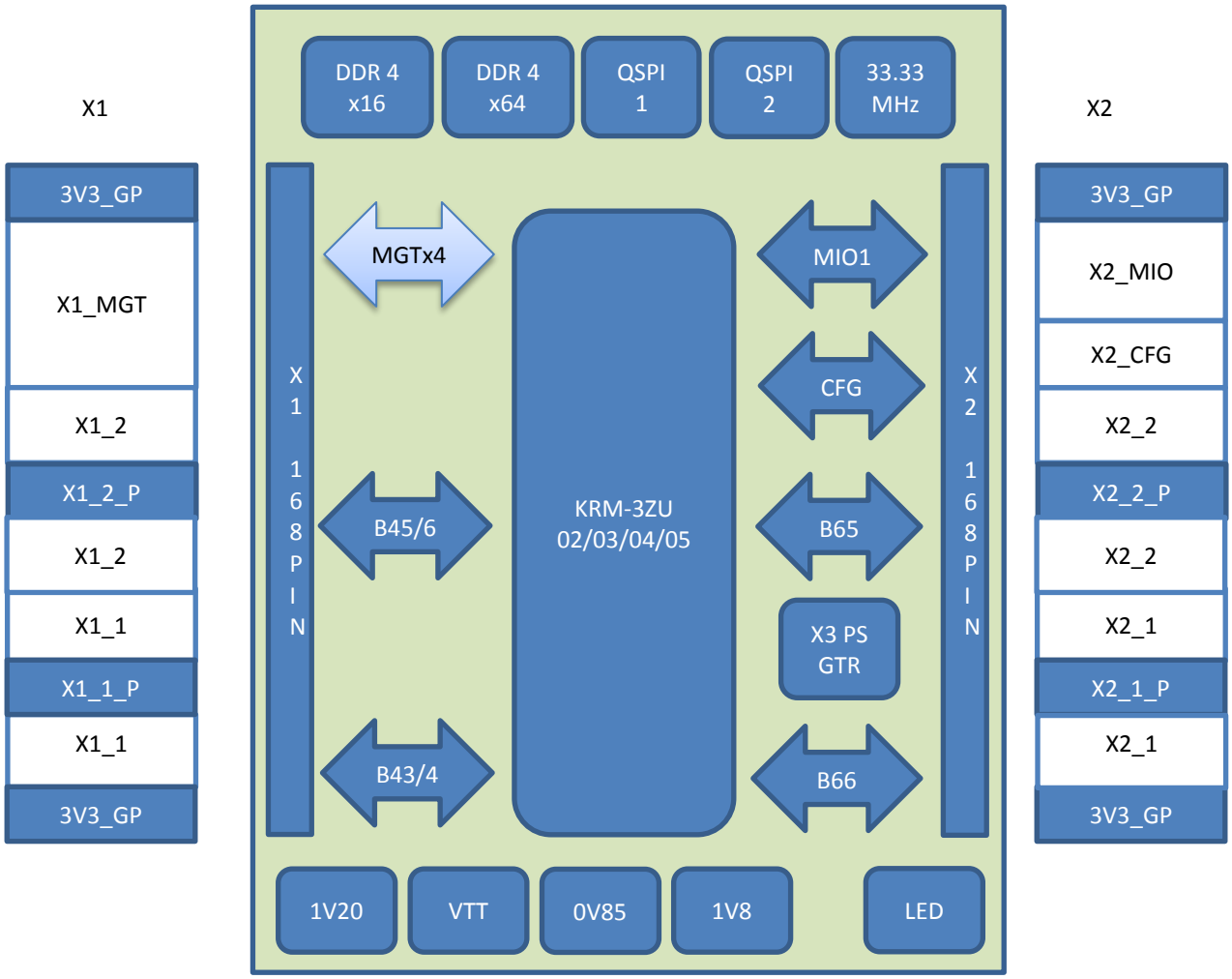
Further support to aid in customer specific design in's is available at competitive rates, please contact KR for details: + 41 61 545 2080 or mail to office@knowres.com

Introduction

With the KRM-3ZUXX, KR provides a highly flexible and cost-efficient board for FPGA and embedded systems prototyping. Due to its low cost, the KRM-3ZUXX is also suitable for integration in low to mid volume end-products. It is based on a Xilinx Zynq Ultrascale+ ™ MPSoC. The Xilinx SoC is accompanied by a 64 bit wide DDR4 memory subsystem on the PS and a 16-bit wide DDR4 memory on the PL, two instances of Quad SPI memory, power regulation, clock sources and 4 user LED.

The modules form-factor and pin assignment is a superset of the Zynq 7000 series based KRM-3Z0xx range and fully backwards compatible with all members of the Zynq 7000 series modules form KR. The modules form factor is 50mm x 70mm x 11mm (with heat spreader), 21W maximum Module power, and the standard pin out.

Block diagram



Board dimensions

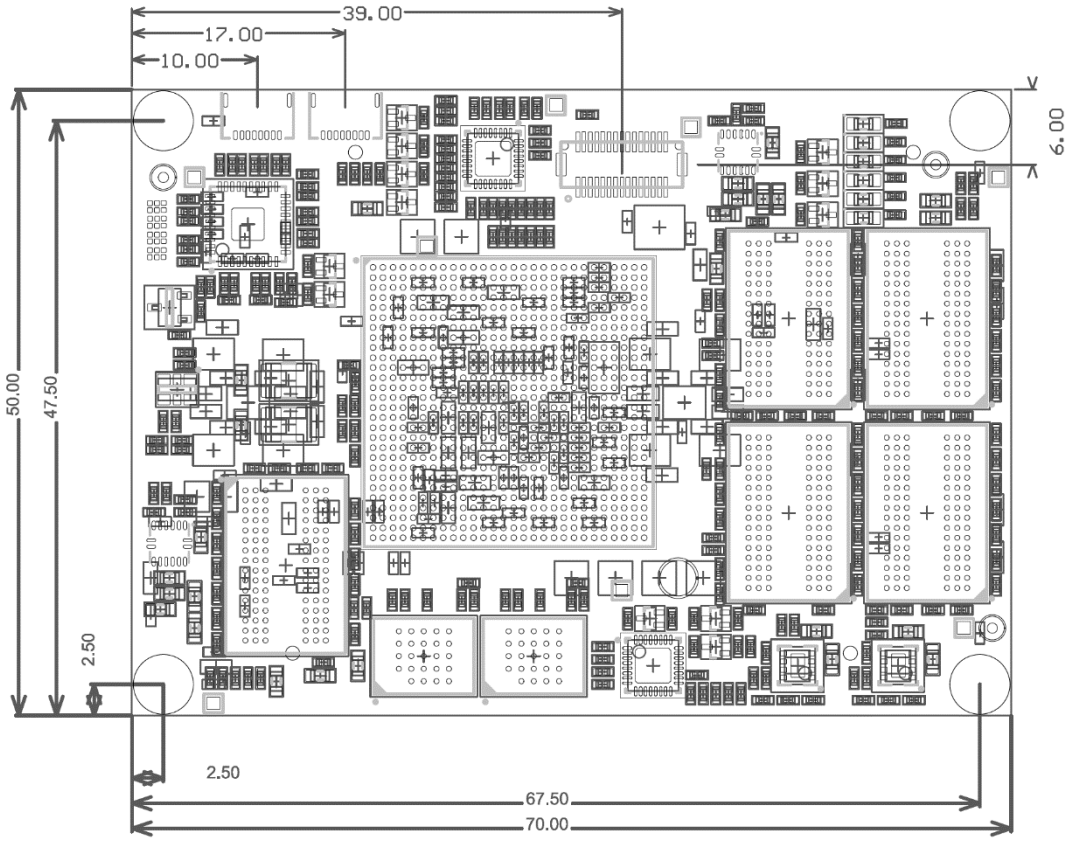


Figure 1: Board dimensions (in mm)

- Step Models of the module and its heat-spreader plate are available
- Altium PCB and Schematic templates are available
-

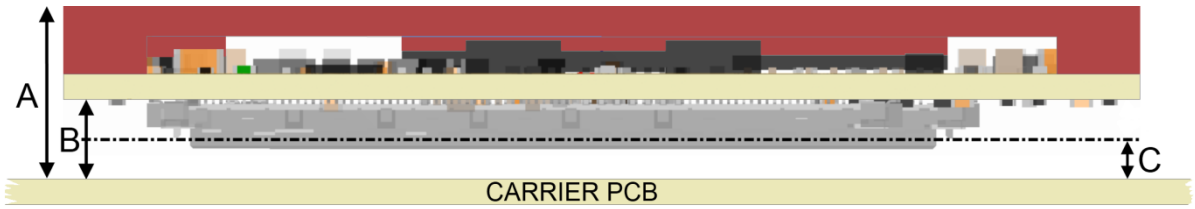


Figure 2: Board to board dimensions

- A = Height above carrier PCB ±0.2mm
- B = Mated stacking height
- C = Maximum component height area of carrier PCB.

Possible header variations:

– FX10A-168P-SV(85)	A = 10mm	B = 4mm	C = 1.5mm
– FX10A-168P-SV1(85)*	A = 11mm	B = 5mm	C = 2.5mm
– FX10A-168P-SV2(85)	A = 12mm	B = 6mm	C = 3.5mm
– FX10A-168P-SV3(85)	A = 13mm	B = 7mm	C = 4.5mm
– FX10A-168P-SV4(85)	A = 14mm	B = 8mm	C = 5.5mm

*KRC3701_CARRIER

Features

Overview

- **Xilinx XCZUxx-xSFVC784E/I**
  - Available in speed grades 1 through 3; Extended or Industrial temperature range as options
  - 47’232 to 117’120 LUTs
  - 94’464 to 243’240 Flip-Flops
  - 240 to 1248 DSP Slices
  - 128 to 216 x 36Kb block RAMs
  - 48 to 64 288KbUltra RAM instances
  - Dual or Quad core 64 bit ARM A53
  - Dual core 32 bit ARM R5
  - MALI GPU
  - 256kB OC-RAM
  - 1M L2 cache

- 2GB to 8GB of 64 bit wide DDR4 SDRAM PS memory
- 512MB of 16 bit wide DDR4 SDRAM PL memory

- 512Mbit QUAD SPI Flash; 2 times 256Mbit, larger densities as options

- 2x 168 pin Hirose FX10 dual row connectors
  - 4x PL I/O bank (Banks 43/44, 45/46, 65, 66)
    - 48 pins each
    - All byte groups (0-3) intact and length matched
    - I/O voltage supplied by carrier board, can be different for each bank
    - External I/O Voltage is switched; switch is enabled by on-board CFG-done signal
  - 1x PS MIO50x bank
    - 1V8 default, supplied by KRM on-board regulator
  - JTAG chain to FPGA; 3V3
  - PS reset in pin
  - Configuration_OK pin; buffered open collector output

- 33.333 MHz on-board oscillator
- 4x Low jitter clock synthesizer for PS transceivers and PL MGTs
- 4 User LED driven by bank 65 (not part of byte groups on I/O connector)
- PL GTH : 4 lanes + 2 external reference clock inputs (only on ZU04 and ZU05)
- PS GTR : 4 transceivers on X600 with on board clock synthesizer plus one external reference input
- On-board programmable clock module

Power supply and power considerations

Core power

-The KRM-3ZUXX requires a **stable** power supply of 3V3. In order to support designs with high FPGA utilization, a supply capable of providing at least 6A is required, 8A is recommended.

-Each of the 4 pin-groups of the 3V3 Global supply must be bypassed with a minimum of 47uF on the carrier board.

-Each Bank I/O supply must be bypassed with a minimum of 47uF on the carrier board.

I/O Bank Power sequence

I/O Bank power is to be supplied by the user design on the carrier board and may range from 1V35 to 3V3 for high-density banks or 1V35 to 1V8 for high-performance banks. Each I/O bank may be powered by a different I/O voltage, for maximum flexibility of the module.
In order to ensure optimal power sequencing of the power rails as recommended by Xilinx, the I/O Bank power is switched by on-board FET so that the user does not have to be concerned about the power sequencing of I/O voltages. The power-up of the I/O banks can be enabled by the "Pok" of the on board regulators or the "config-done" of the FPGA (an assembly option on the module).
The default power on of the I/O power rails is driven by the signal that indicates the completion of the FPGA configuration.

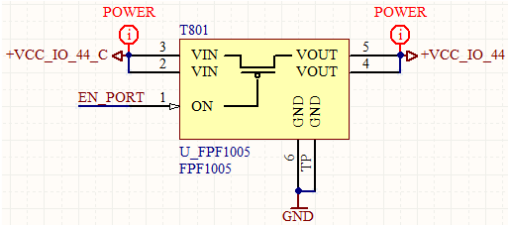


Figure 3:

Supply Type	FX10 pin number	Voltage	Current	Remark
Global Module supply for internal regulators and CFG circuits	X1: 1,2, 165,166,167,168[i] X2: 1,2,3,4,165,166,167,168	3V3 Global	4.2A [ii]	Bypass each corner with at least 47uF on carrier
I/O Supply X1 GROUP1 (BANK 46 & 45)	X1:29,30	1V35 to 3V3	600mA [iii]	Bypass with at least 47uF on carrier
I/O Supply X1 GROUP2 (BANK 43 & 44)	X1:83,84	1V35 to 3V3	600mA	Bypass with at least 47uF on carrier
I/O Supply X2 GROUP1 (BANK 65)	X2: 31,32	1V35 to 1V8	600mA	Bypass with at least 47uF on carrier
I/O Supply X2 GROUP2 (BANK 66)	X2: 85,86	1V35 to 1V8	600mA	Bypass with at least 47uF on carrier

[i] In order to ensure best performance with MGT capable modules, treat X1: 165-168 as low noise supply pins and isolate with a ferrite bead /capacitor Pi filter from other 3V3 rails.
[ii] The maximum core power to the Module is 14x 0.3A @3.3V = 13.86W.
[iii] The maximum I/O power to the module is 4x 0.6A @3.3V = 7.92W

Clocking resources

Onboard oscillator

The onboard oscillator provides 33.33 MHz to the PS PLL of the SoC.

External PL Fabric clocks

Each bank exposes all clock capable pins, please consult the I/O tables and Xilinx clocking guide for details.

External MGT clocks

Two MGT clock inputs are provided through the FX10 connector interface.

Reset

-The PS reset port is available in the configuration and housekeeping signal group on connector X2: Pin115
-The reset pin is internally pulled up to 3V3 Global and forwarded to the PS reset pin via the BMC.
-Power-on-reset (PoR) is available via HW_RESET_IN on connector X2: Pin125.
-The module is kept in hardware reset until all voltages are stable.
-The module is self-resetting at power up, no external reset or power monitor is required or recommended.
-Unless there is an explicit need for a HW reset capability, tie pin X2:125 to GND.
-Reset_INn is best left unconnected or driven by an open drain source such as a JTAG adapter.

Signal name	FPGA pin	Board connector	Direction	Remark	I/O Level
RESET_INn	NA	X2: Pin115	FX10 → BMC ->FPGA	active low	INT PU to 3V3
HW_RESET_IN	NA	X2: Pin125	FX10 ->BMC -> FPGA	active high	3V3

Ready

-The module reports the conclusion of the configuration process via the signal CFG_OKn on connector X2:Pin116.
-CFG_OKn is a connected to a dedicated FET and implemented as an open drain output. It may sink as much as 50mA. An external pull-up resistor is required.
-CFG_OKn is provided by the BMC controller and derived from the Config-Done signal of the FPGA.
-CFG_OKn goes low after the FPGA/SoC has been configured successfully.

Signal name	FPGA pin	Board connector	Direction	Remark	I/O Level
CFG_OKn	NA	X2: Pin116	FPGA→ BMC -> FX10	active low	OC

VCC_PSBATT

The VCC_PSBATT input is available via V_BATT_IN on connector X2: Pin126.

Signal name	FPGA pin	Board connector	Direction	Remark	I/O Level
V_BATT_IN	Y18	X2: Pin126	X2 -> FPGA	active high	2V max

Configuration

JTAG Interface

The FPGA configuration file - i.e. the FPGA firmware - can be loaded via dedicated JTAG pins

	Signal name	Board connector	Direction	Remark	I/O Level
JTAG	TMS	X2:118	FX10 → FPGA		3V3
	TCK	X2:117	FX10 → FPGA		3V3
	TDO	X2:120	FPGA → FX10		3V3
	TDI	X2:119	FX10 → FPGA		3V3

Mode Pins

The mode pins of the MPSoC are controlled via persistent settings on the Board Management Controller. It is possible to modify the boot source sending the appropriate commands to the BMC through a serial connection. Please, refer to the document entitled *BMC_how_to_guide.pdf* for more information.

On-Board Quad SPI Configuration Memory

Two instances of QSPI memory are implemented on the module.

Each instance is populated with a 512Mbit (or larger) QSPI flash.

	Signal name	MIO	Direction	Remark	I/O Level
QSPI Flash (U400)	CSn	B500_MIO.07	FPGA → QSPI Flash	Pull up on Module	3V3
	SCK	B500_MIO.12	FPGA → QSPI Flash		3V3
	HOLDn/IO3	B500_MIO.11	BI-DIR	Pull up on Module	3V3
	WPn/IO2	B500_MIO.10	BI-DIR		3V3
	SO/IO1	B500_MIO.09	BI-DIR		3V3
	SI/IO0	B500_MIO.08	BI-DIR		3V3

	Signal name	MIO	Direction	Remark	I/O Level
QSPI Flash (U401)	CSn	B500_MIO.05	FPGA → QSPI Flash	Pull up on Module	3V3
	SCK	B500_MIO.00	FPGA → QSPI Flash		3V3
	HOLDn/IO3	B500_MIO.03	BI-DIR	Pull up on Module	3V3
	WPn/IO2	B500_MIO.02	BI-DIR		3V3
	SO/IO1	B500_MIO.01	BI-DIR		3V3
	SI/IO0	B500_MIO.04	BI-DIR		3V3

DDR4 SDRAM

-The KRM-3ZUXX P**S** memory is populated with four 16 bit wide DDR4 SDRAM chips with a density of 4 to 16Gbit each resulting in a total of 2/4/8GB of RAM operating at 2.4GT/s with 64 bit of width.

-The KRM-3ZUXX P**L** memory is populated with one 16 bit wide DDR4 SDRAM with a density of 4/8/16Gbit.
-The PL Memory subsystem can run as fast as 2666MT/s on a -3 part, 2400MT/s are standard on all speed grades.

A reference design based on the Xilinx MIG core is available to demonstrate the performance of the PL DDR4 memory of the module.

PS GTR CONNECTOR

In order to be fully backwards compatible, with the previous 7000 series based modules, the new PS GTR transceivers of the MPSoC based modules are not mapped onto the PL MGT transceiver positions of X1, but are placed on a new DF12 30-pin connector (X600) on top of the module. Due to the rather limited speed of 6Gbs, those signals can be connected to a dedicated I/O board or carrier via GND referenced flex PCB.
In addition to the PS transceiver signals, bit 12 of the four byte-lanes of Bank 66 are also mapped to the connector. The I/O level is defined by the voltage applied to Bank 66 and supports a maximum of 1V8. Use those signals to implement support signaling for high-speed differential I/O's, i.e.:

- The AUX channel for Display Port,
- The over-current detect for USB interfaces,
- Signaling of link status.

B66.T0_12 is also the VRP signal if that bank is to be used with DCI I/O standards. If the module is ordered with DCI enabled for Bank 66, that signal is not available for user I/O and must remain unconnected.

	Signal name	PIN	Direction	Remark	I/O Level
PS GTR (X600)	B66.T3 12	1	Bidirectional		1V8 MAX
	B66.T2 12	2	Bidirectional		1V8 MAX
	B66.T1 12	3	Bidirectional		1V8 MAX
	B66.T0 12	4	Bidirectional	Optional VRP for B66	1V8 MAX
	GND	5			
	GND	6			
	PS_MGT_TX.03_P	7	FPGA -> X5		
	PS_MGT_RX.03_P	8	X5 -> FPGA		
	PS_MGT_TX.03_N	9	FPGA -> X5		
	PS_MGT_RX.03_N	10	X5 -> FPGA		
	GND	11			
	GND	12			
	PS_MGT_TX.02_P	13	FPGA -> X5		
	PS_MGT_RX.02_P	14	X5 -> FPGA		
	PS_MGT_TX.02_N	15	FPGA -> X5		
	PS_MGT_RX.02_N	16	X5 -> FPGA		
	GND	17			
	GND	18			
	PS_MGT_TX.01_P	19	FPGA -> X5		
	PS_MGT_RX.01_P	20	X5 -> FPGA		
	PS_MGT_TX.01_N	21	FPGA -> X5		
	PS_MGT_RX.01_N	22	X5 -> FPGA		
	GND	23			
	GND	24			
	PS_MGT_TX.00_P	25	FPGA -> X5		
	PS_MGT_RX.00_P	26	X5 -> FPGA		
	PS_MGT_TX.00_N	27	FPGA -> X5		
	PS_MGT_RX.00_N	28	X5 -> FPGA		
	GND	29			
	GND	30			

PS GTR NOTES

- The transceiver signals are DC coupled, any AC coupling MUST be implemented in the user design
- The reference clocks for the four transceivers are generated by the on board clock synthesizer
  - Frequencies can be configured by loading a clock synthesizer configuration file into the BMC via the BMC UART. See clock generator user guide for details.
  - The frequencies can be synthesized free running off the on-board clock source or derived from one of the two MGT clock inputs on X1
  - The clock inputs on X1 *can* now serve as the reference clock for all on module needs, in the following way:
    - Direct pass through to any of the 6 transceiver reference inputs
    - Divided pass through to any of the 6 transceiver reference inputs
    - Source clock for the PLL and synthesizer stage of the clock synthesizer SI5332

I/O Headers

The KRM-3ZUXX s I/O pinning is fully compatible with all future and past releases of KRM-3 series modules.
Two Hirose FX10 168 pin connectors provide a total of 192 PL I/O signals, 38 PS MIO signals, 4MGT lanes,
2 differential MGT reference clocks, configuration and status pins.
Matching connectors for the carrier board design are:

- FX10A-168P-SVx

Please note HIROSE annotation is Pin **1a to 84a** and **1b to 84b**
This corresponds to KR annotation Pin **1 to 167** and **2 to 168**

	Group	FPGA Bank	Remark	I/O Level
X1	X1_1	Bank 46/45	3V3 or below HD	3V3 to 1V35
	X1_2	Bank 43/44	3V3 or below HD	3V3 to 1V35
	X1_MGT	x8		

	Group	FPGA Bank	Remark	I/O Level
X2	X2_1	Bank 65	1V8 MAX HP	1V8 to 1V35
	X2_2	Bank 66	1V8 MAX HP	1V8 to 1V35
	X2_CFG	CFG		3V3
	X2_MIO	MIO 501 & 502	1V8 default	1V8/3V3

PL BANKS

- The Byte-groups of a PL I/O bank (T0 –T3) are kept as a group and are length matched on the module.
- Differential I/O capable pins of the PL are routed as loosely coupled differential pairs.

The I/O headers X1 and X2 feature I/O groups that are the same on all KRM-3ZUXX modules. The I/O groups are the same for each module of the KRM-3ZUXX family but each module may map different ports to the I/O groups. In order to be fully compatible with all currently planned KRM-3ZUXX compliant modules, the X2 I/O banks should only use I/O voltages of 1V8 or less as some Modules will map **High performance** banks instead of **High range** banks onto X2.
The I/O banks on X2 of the KRM-3ZUXX module are High performance (HP) banks and may only use supply voltages up to 1V8.

MIO BANK

1V8 is the default I/O voltage.
MIO signals below are available:

- Bank 501: MIO26 to MIO37,
- Bank 501: MIO40 to MIO41,
- Bank 501: MIO44 to MIO51,

- Bank 502: MIO52 to MIO63,
- Bank 502: MIO74 to MIO77.

In order to be compatible with KR issued Linux BSP's we recommend using the MIO assignment as shown on one of the KR issued Evaluation boards such as the KRC3701 carrier.
Naturally other configurations are possible, contact KR for BSP support of your desired configuration.

MGT BANK

4 of 8 MGT lanes are available on the MGT block of X1. Two external reference clock(s) may be applied so that the module can simultaneously support MGT standards that are based on one or two different clock reference. The clock signals are AC coupled on the module and do *not* require AC coupling on the carrier.
As the MGT reference clocks feed a clock synthesizer, they can also be used as sources for any of the 4 PS transceivers.

Connector Schematic

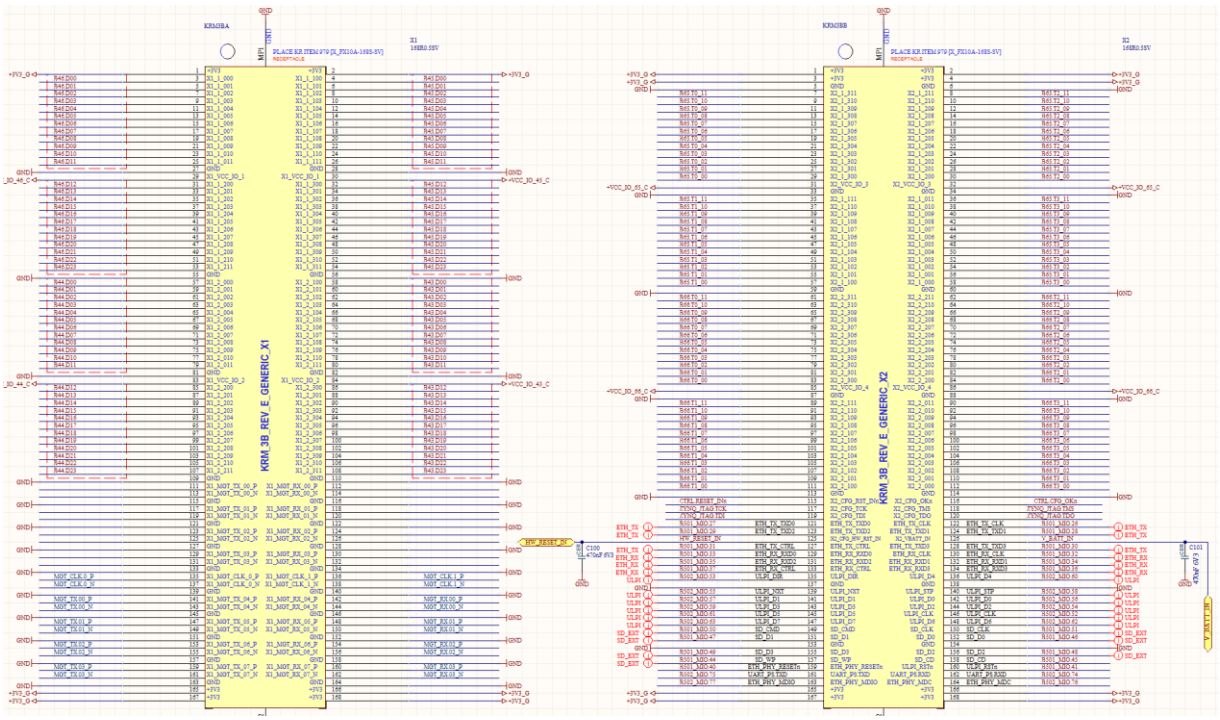


Figure 5:

Changes to prior module generations

X2 Pin 126 was assigned to GND in the original release of the KRM-3 Module family
As of PCB REV E of the Zynq 7000 series modules and all MPSoC based KRM-3 Modules, this pin is internally connected to the VCC_PSBATT pin of the FPGA. The newer modules are fully backwards compatible with carriers that implement GND on that pin. However the battery backed keeping of encryption keys is not supported on older carriers.

X2 pin 125 was assigned to GND in the original release of the KRM-3 Module family
As of PCB REV E of the Zynq 7000 series modules and all MPSoC based KRM-3 Modules, this pin is internally connected to HW Reset. This signal is active HIGH and will trigger a fresh configuration cycle. Due to the signal polarity, the new modules are fully backwards compatible with carriers that implement GND on this pin. The external HW reset is not available if the module is installed on older carriers that do not offer the HW reset signal.

User LED and DCI for HP I/O banks
The module may be ordered with DCI enabled (240R resistors to GND on VRP which is on B65.T0_12 and B66.T0_12). With those options active User LED D4 (bottom of the stack) is no longer available as the same pin would be used to drive the LED. Furthermore one of the I/O's on the PS MGT connector is also not available.

Pin Mapping

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
NA	NA	U12	DXN	NA	NA	CONFIG	NA	GND	GND
VCCADC	NA	P12	VCCADC	NA	NA	CONFIG	NA	+1V8_VCC_AUX	+1V8
GNDADC	NA	P13	GNDADC	NA	NA	CONFIG	NA	GND	GND
NA	NA	U13	DXP	NA	NA	CONFIG	NA	GND	GND
NA	NA	T13	VREFP	NA	NA	CONFIG	NA	GND	GND
NA	NA	R12	VREFN	NA	NA	CONFIG	NA	GND	GND
NA	NA	R13	VP	NA	NA	CONFIG	NA	NA	NA
NA	NA	T12	VN	NA	NA	CONFIG	NA	NA	NA
PUDC_B	NA	U7	PUDC_B	NA	0	CONFIG	NA	+1V8_VCC_AUX	+1V8
POR_OVERRIDE	NA	W7	POR_OVERRIDE	NA	NA	NA	NA	GND	GND
PL_IO	X1:53	L13	IO_L12N_AD0N	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:51	L14	IO_L12P_AD0P	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:49	J14	IO_L11N_AD1N	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:47	K14	IO_L11P_AD1P	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:45	H13	IO_L10N_AD2N	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:43	H14	IO_L10P_AD2P	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:41	G14	IO_L9N_AD3N	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:39	G15	IO_L9P_AD3P	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:37	E15	IO_L8N_HDGC_AD4N	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:35	F15	IO_L8P_HDGC_AD4P	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:33	F13	IO_L7N_HDGC_AD5N	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:31	G13	IO_L7P_HDGC_AD5P	2	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:25	E13	IO_L6N_HDGC_AD6N	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:23	E14	IO_L6P_HDGC_AD6P	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:21	D14	IO_L5N_HDGC_AD7N	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:19	D15	IO_L5P_HDGC_AD7P	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:17	C13	IO_L4N_AD8N	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:15	C14	IO_L4P_AD8P	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:13	A13	IO_L3N_AD9N	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:11	B13	IO_L3P_AD9P	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:9	A14	IO_L2N_AD10N	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:7	B14	IO_L2P_AD10P	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:5	A15	IO_L1N_AD11N	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:3	B15	IO_L1P_AD11P	0	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 46 XCZU3/2 : 26
PL_IO	X1:54	C12	IO_L12N_AD8N	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	X1:52	D12	IO_L12P_AD8P	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:50	A11	IO_L11N_AD9N	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:48	A12	IO_L11P_AD9P	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:46	A10	IO_L10N_AD10N	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:44	B11	IO_L10P_AD10P	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:42	B10	IO_L9N_AD11N	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:40	C11	IO_L9P_AD11P	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:38	D11	IO_L8N_HDGC	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:36	E12	IO_L8P_HDGC	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:34	D10	IO_L7N_HDGC	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:32	E10	IO_L7P_HDGC	3	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:26	F11	IO_L6N_HDGC	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:24	F12	IO_L6P_HDGC	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:22	F10	IO_L5N_HDGC	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:20	G11	IO_L5P_HDGC	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:18	H12	IO_L4N_AD12N	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:16	J12	IO_L4P_AD12P	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:14	G10	IO_L3N_AD13N	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:12	H11	IO_L3P_AD13P	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:10	K12	IO_L2N_AD14N	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:8	K13	IO_L2P_AD14P	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:6	J10	IO_L1N_AD15N	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:4	J11	IO_L1P_AD15P	1	See Remark	HD	X1_1	VIO_X1_1	XCZU5/4 : 45 XCZU3/2 : 25
PL_IO	X1:107	AA12	IO_L12N_AD8N_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:105	Y12	IO_L12P_AD8P_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:103	W11	IO_L11N_AD9N_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:101	W12	IO_L11P_AD9P_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:99	Y13	IO_L10N_AD10N_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:97	Y14	IO_L10P_AD10P_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:95	W13	IO_L9N_AD11N_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:93	W14	IO_L9P_AD11P_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:91	AB14	IO_L8N_HDGC_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:89	AB15	IO_L8P_HDGC_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:87	AB13	IO_L7N_HDGC_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:85	AA13	IO_L7P_HDGC_24	2	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:79	AC13	IO_L6N_HDGC_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	X1:77	AC14	IO_L6P_HDGC_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:75	AD14	IO_L5N_HDGC_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:73	AD15	IO_L5P_HDGC_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:71	AF13	IO_L4N_AD12N_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:69	AE13	IO_L4P_AD12P_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:67	AH13	IO_L3N_AD13N_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:65	AG13	IO_L3P_AD13P_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:63	AH14	IO_L2N_AD14N_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:61	AG14	IO_L2P_AD14P_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:59	AE14	IO_L1N_AD15N_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:57	AE15	IO_L1P_AD15P_24	0	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 44 XCZU3/2 : 24
PL_IO	X1:108	AB9	IO_L12N_AD0N_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:106	AB10	IO_L12P_AD0P_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:104	AA8	IO_L11N_AD1N_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:102	Y9	IO_L11P_AD1P_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:100	Y10	IO_L10N_AD2N_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:98	W10	IO_L10P_AD2P_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:96	AA10	IO_L9N_AD3N_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:94	AA11	IO_L9P_AD3P_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:92	AC11	IO_L8N_HDGC_AD4N_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:90	AB11	IO_L8P_HDGC_AD4P_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:88	AD10	IO_L7N_HDGC_AD5N_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:86	AD11	IO_L7P_HDGC_AD5P_44	3	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:80	AD12	IO_L6N_HDGC_AD6N_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:78	AC12	IO_L6P_HDGC_AD6P_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:76	AF12	IO_L5N_HDGC_AD7N_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:74	AE12	IO_L5P_HDGC_AD7P_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:72	AF10	IO_L4N_AD8N_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:70	AE10	IO_L4P_AD8P_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:68	AH11	IO_L3N_AD9N_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:66	AH12	IO_L3P_AD9P_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:64	AG11	IO_L2N_AD10N_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:62	AF11	IO_L2P_AD10P_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:60	AH10	IO_L1N_AD11N_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X1:58	AG10	IO_L1P_AD11P_44	1	See Remark	HD	X1_2	VIO_X1_2	XCZU5/4 : 43 XCZU3/2 : 44
PL_IO	X2:90	B9	IO_L24N_T3U_N11_66	0	66	HP	X2_2	VIO_X2_2	

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	X2:92	C9	IO_L24P_T3U_N10_66	0	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:94	A8	IO_L23N_T3U_N9_66	0	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:96	A9	IO_L23P_T3U_N8_66	0	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:98	B8	IO_L22N_T3U_N7_DBC_AD0N_66	0	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:100	C8	IO_L22P_T3U_N6_DBC_AD0P_66	0	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:102	A6	IO_L21N_T3L_N5_AD8N_66	0	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:104	A7	IO_L21P_T3L_N4_AD8P_66	0	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:106	B6	IO_L20N_T3L_N3_AD1N_66	0	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:108	C6	IO_L20P_T3L_N2_AD1P_66	0	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:110	A5	IO_L19N_T3L_N1_DBC_AD9N_66	0	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:112	B5	IO_L19P_T3L_N0_DBC_AD9P_66	0	66	HP	X2_2	VIO_X2_2	
PL_IO	X600:1	C7	IO_T3U_N12_66	NA	66	HP	NA	NA	
PL_IO	X600:2	E7	IO_T2U_N12_66	NA	66	HP	NA	NA	
PL_IO	X2:62	D9	IO_L18N_T2U_N11_AD2N_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:64	E9	IO_L18P_T2U_N10_AD2P_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:66	E8	IO_L17N_T2U_N9_AD10N_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:68	F8	IO_L17P_T2U_N8_AD10P_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:70	F7	IO_L16N_T2U_N7_QBC_AD3N_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:72	G8	IO_L16P_T2U_N6_QBC_AD3P_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:74	F6	IO_L15N_T2L_N5_AD11N_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:76	G6	IO_L15P_T2L_N4_AD11P_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:78	D5	IO_L14N_T2L_N3_GC_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:80	E5	IO_L14P_T2L_N2_GC_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:82	D6	IO_L13N_T2L_N1_GC_QBC_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:84	D7	IO_L13P_T2L_N0_GC_QBC_66	2	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:89	C2	IO_L12N_T1U_N11_GC_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:91	C3	IO_L12P_T1U_N10_GC_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:93	C4	IO_L11N_T1U_N9_GC_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:95	D4	IO_L11P_T1U_N8_GC_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:97	A4	IO_L10N_T1U_N7_QBC_AD4N_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:99	B4	IO_L10P_T1U_N6_QBC_AD4P_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:101	A3	IO_L9N_T1L_N5_AD12N_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:103	B3	IO_L9P_T1L_N4_AD12P_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:105	A1	IO_L8N_T1L_N3_AD5N_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:107	A2	IO_L8P_T1L_N2_AD5P_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:109	B1	IO_L7N_T1L_N1_QBC_AD13N_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:111	C1	IO_L7P_T1L_N0_QBC_AD13P_66	1	66	HP	X2_2	VIO_X2_2	
PL_IO	X600:3	D2	IO_T1U_N12_66	NA	66	HP	NA	NA	
PL_IO	X600:4	G4	IO_T0U_N12_VRP_66	NA	66	HP	NA	NA	
PL_IO	X2:61	F5	IO_L6N_T0U_N11_AD6N_66	3	66	HP	X2_2	VIO_X2_2	

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	X2:63	G5	IO_L6P_T0U_N10_AD6P_66	3	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:65	E3	IO_L5N_T0U_N9_AD14N_66	3	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:67	E4	IO_L5P_T0U_N8_AD14P_66	3	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:69	F3	IO_L4N_T0U_N7_DBC_AD7N_66	3	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:71	G3	IO_L4P_T0U_N6_DBC_AD7P_66	3	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:73	E2	IO_L3N_T0L_N5_AD15N_66	3	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:75	F2	IO_L3P_T0L_N4_AD15P_66	3	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:77	D1	IO_L2N_T0L_N3_66	3	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:79	E1	IO_L2P_T0L_N2_66	3	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:81	F1	IO_L1N_T0L_N1_DBC_66	3	66	HP	X2_2	VIO_X2_2	
PL_IO	X2:83	G1	IO_L1P_T0L_N0_DBC_66	3	66	HP	X2_2	VIO_X2_2	
PL_VREF	NA	G9	VREF_66	NA	66	HP	NA	NA	GND
PL_IO	X2:36	H8	IO_L24N_T3U_N11_PERSTN0_65	0	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:38	H9	IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65	0	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:40	J9	IO_L23N_T3U_N9_65	0	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:42	K9	IO_L23P_T3U_N8_I2C_SCLK_65	0	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:44	K7	IO_L22N_T3U_N7_DBC_AD0N_65	0	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:46	K8	IO_L22P_T3U_N6_DBC_AD0P_65	0	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:48	H7	IO_L21N_T3L_N5_AD8N_65	0	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:50	J7	IO_L21P_T3L_N4_AD8P_65	0	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:52	H6	IO_L20N_T3L_N3_AD1N_65	0	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:54	J6	IO_L20P_T3L_N2_AD1P_65	0	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:56	J4	IO_L19N_T3L_N1_DBC_AD9N_65	0	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:58	J5	IO_L19P_T3L_N0_DBC_AD9P_65	0	65	HP	X2_1	VIO_X2_1	
PL_RAM_RST_N	NA	K5	IO_T3U_N12_65	NA	65	HP	NA	NA	LED D500 OFF when PL_RAM_RST_N active
LED_D501	NA	P9	IO_T2U_N12_65	NA	65	HP	NA	NA	USER_LED_D501
PL_IO	X2:8	L8	IO_L18N_T2U_N11_AD2N_65	2	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:10	M8	IO_L18P_T2U_N10_AD2P_65	2	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:12	N8	IO_L17N_T2U_N9_AD10N_65	2	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:14	N9	IO_L17P_T2U_N8_AD10P_65	2	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:16	P6	IO_L16N_T2U_N7_QBC_AD3N_65	2	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:18	P7	IO_L16P_T2U_N6_QBC_AD3P_65	2	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:20	N6	IO_L15N_T2L_N5_AD11N_65	2	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:22	N7	IO_L15P_T2L_N4_AD11P_65	2	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:24	L5	IO_L14N_T2L_N3_GC_65	2	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:26	M6	IO_L14P_T2L_N2_GC_65	2	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:28	L6	IO_L13N_T2L_N1_GC_QBC_65	2	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:30	L7	IO_L13P_T2L_N0_GC_QBC_65	2	65	HP	X2_1	VIO_X2_1	

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	X2:35	L2	IO_L12N_T1U_N11_GC_65	1	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:37	L3	IO_L12P_T1U_N10_GC_65	1	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:39	K3	IO_L11N_T1U_N9_GC_65	1	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:41	K4	IO_L11P_T1U_N8_GC_65	1	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:43	H3	IO_L10N_T1U_N7_QBC_AD4N_65	1	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:45	H4	IO_L10P_T1U_N6_QBC_AD4P_65	1	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:47	J2	IO_L9N_T1L_N5_AD12N_65	1	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:49	K2	IO_L9P_T1L_N4_AD12P_65	1	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:51	H1	IO_L8N_T1L_N3_AD5N_65	1	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:53	J1	IO_L8P_T1L_N2_AD5P_65	1	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:55	K1	IO_L7N_T1L_N1_QBC_AD13N_65	1	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:57	L1	IO_L7P_T1L_N0_QBC_AD13P_65	1	65	HP	X2_1	VIO_X2_1	
LED_D502	NA	H2	IO_T1U_N12_65	NA	65	HP	NA	NA	USER_LED_D502
LED_D503	NA	W9	IO_T0U_N12_VRP_65	NA	65	HP	NA	NA	USER_LED_D503
PL_IO	X2:7	T6	IO_L6N_T0U_N11_AD6N_65	3	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:9	R6	IO_L6P_T0U_N10_AD6P_65	3	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:11	T7	IO_L5N_T0U_N9_AD14N_65	3	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:13	R7	IO_L5P_T0U_N8_AD14P_65	3	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:15	T8	IO_L4N_T0U_N7_DBC_AD7N_65	3	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:17	R8	IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65	3	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:19	V8	IO_L3N_T0L_N5_AD15N_65	3	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:21	U8	IO_L3P_T0L_N4_AD15P_65	3	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:23	V9	IO_L2N_T0L_N3_65	3	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:25	U9	IO_L2P_T0L_N2_65	3	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:27	Y8	IO_L1N_T0L_N1_DBC_65	3	65	HP	X2_1	VIO_X2_1	
PL_IO	X2:29	W8	IO_L1P_T0L_N0_DBC_65	3	65	HP	X2_1	VIO_X2_1	
PL_VREF	NA	R9	VREF_65	NA	65	HP	NA	NA	GND
PL_RAM	NA	AG1	IO_L24N_T3U_N11_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_LDQ4
PL_RAM	NA	AF1	IO_L24P_T3U_N10_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_LDQ2
PL_RAM	NA	AH1	IO_L23N_T3U_N9_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_LDQ0
PL_RAM	NA	AH2	IO_L23P_T3U_N8_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_LDQ6
PL_RAM	NA	AF2	IO_L22N_T3U_N7_DBC_AD0N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_LDQS_c
PL_RAM	NA	AE2	IO_L22P_T3U_N6_DBC_AD0P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_LDQS_t
PL_RAM	NA	AF3	IO_L21N_T3L_N5_AD8N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_LDQ3
PL_RAM	NA	AE3	IO_L21P_T3L_N4_AD8P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_LDQ1
PL_RAM	NA	AH3	IO_L20N_T3L_N3_AD1N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_LDQ7
PL_RAM	NA	AG3	IO_L20P_T3L_N2_AD1P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_LDQ5
PL_RAM	NA	AH4	IO_L19N_T3L_N1_DBC_AD9N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_ODT
PL_RAM	NA	AG4	IO_L19P_T3L_N0_DBC_AD9P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_LDM

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_RAM	NA	AE4	IO_T3U_N12_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A12/BC_n
PL_RAM	NA	AB5	IO_T2U_N12_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_CS_n
PL_RAM	NA	AC1	IO_L18N_T2U_N11_AD2N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_UDQ2
PL_RAM	NA	AB1	IO_L18P_T2U_N10_AD2P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_UDQ0
PL_RAM	NA	AC2	IO_L17N_T2U_N9_AD10N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_UDQ6
PL_RAM	NA	AB2	IO_L17P_T2U_N8_AD10P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_UDQ4
PL_RAM	NA	AD1	IO_L16N_T2U_N7_QBC_AD3N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_UDQS_c
PL_RAM	NA	AD2	IO_L16P_T2U_N6_QBC_AD3P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_UDQS_t
PL_RAM	NA	AB3	IO_L15N_T2L_N5_AD11N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_UDQ1
PL_RAM	NA	AB4	IO_L15P_T2L_N4_AD11P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_UDQ3
PL_RAM	NA	AC3	IO_L14N_T2L_N3_GC_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_UDQ7
PL_RAM	NA	AC4	IO_L14P_T2L_N2_GC_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_UDQ5
PL_RAM	NA	AD4	IO_L13N_T2L_N1_GC_QBC_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_RAS_n/A16
PL_RAM	NA	AD5	IO_L13P_T2L_N0_GC_QBC_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_UDM
PL_RAM	NA	AF5	IO_L12N_T1U_N11_GC_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_CKE
PL_RAM	NA	AE5	IO_L12P_T1U_N10_GC_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A3
PL_RAM	NA	AF6	IO_L11N_T1U_N9_GC_64	NA	64	HP	NA	+1V2_VCC_DDR	NA
PL_RAM	NA	AF7	IO_L11P_T1U_N8_GC_64	NA	64	HP	NA	+1V2_VCC_DDR	NA
PL_RAM	NA	AG5	IO_L10N_T1U_N7_QBC_AD4N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_WE_n/A14
PL_RAM	NA	AG6	IO_L10P_T1U_N6_QBC_AD4P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A10/AP
PL_RAM	NA	AH7	IO_L9N_T1L_N5_AD12N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A0
PL_RAM	NA	AH8	IO_L9P_T1L_N4_AD12P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A11
PL_RAM	NA	AG8	IO_L8N_T1L_N3_AD5N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A2
PL_RAM	NA	AF8	IO_L8P_T1L_N2_AD5P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A8
PL_RAM	NA	AH9	IO_L7N_T1L_N1_QBC_AD13N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_CK_c
PL_RAM	NA	AG9	IO_L7P_T1L_N0_QBC_AD13P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_CK_t
PL_RAM	NA	AH6	IO_T1U_N12_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_BA0
PL_VRP	NA	AD6	IO_T0U_N12_VRP_64	NA	64	HP	NA	GND	PULL DOWN
PL_RAM	NA	AC6	IO_L6N_T0U_N11_AD6N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_BG1
PL_RAM	NA	AB6	IO_L6P_T0U_N10_AD6P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_CAS_n/A15
PL_RAM	NA	AC7	IO_L5N_T0U_N9_AD14N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A1
PL_RAM	NA	AB7	IO_L5P_T0U_N8_AD14P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_BA1
PL_RAM	NA	AE7	IO_L4N_T0U_N7_DBC_AD7N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_BG0
PL_RAM	NA	AD7	IO_L4P_T0U_N6_DBC_AD7P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_ACT_n
PL_RAM	NA	AC8	IO_L3N_T0L_N5_AD15N_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A9
PL_RAM	NA	AB8	IO_L3P_T0L_N4_AD15P_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A5
PL_RAM	NA	AE8	IO_L2N_T0L_N3_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A4
PL_RAM	NA	AE9	IO_L2P_T0L_N2_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A6
PL_RAM	NA	AD9	IO_L1N_T0L_N1_DBC_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A7
PL_RAM	NA	AC9	IO_L1P_T0L_N0_DBC_64	NA	64	HP	NA	+1V2_VCC_DDR	U700_A13

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_VREF	NA	AA7	VREF_64	NA	64	HP	NA	+1V2_VCC_DDR	+0.6V
64MB QSPI Flash	NA	AG15	PS_MIO0	NA	500	PSMIO	NA	+3V3_G	L_QSPI_CLK
64MB QSPI Flash	NA	AG16	PS_MIO1	NA	500	PSMIO	NA	+3V3_G	L_QSPI_D1
64MB QSPI Flash	NA	AD17	PS_MIO10	NA	500	PSMIO	NA	+3V3_G	U_QSPI_D2
64MB QSPI Flash	NA	AE17	PS_MIO11	NA	500	PSMIO	NA	+3V3_G	U_QSPI_D3
64MB QSPI Flash	NA	AC17	PS_MIO12	NA	500	PSMIO	NA	+3V3_G	U_QSPI_CLK
NC	NA	AH18	PS_MIO13	NA	500	PSMIO	NA	NA	NC
NC	NA	AG18	PS_MIO14	NA	500	PSMIO	NA	NA	NC
NC	NA	AE18	PS_MIO15	NA	500	PSMIO	NA	NA	NC
NC	NA	AF18	PS_MIO16	NA	500	PSMIO	NA	NA	NC
NC	NA	AC18	PS_MIO17	NA	500	PSMIO	NA	NA	NC
NC	NA	AC19	PS_MIO18	NA	500	PSMIO	NA	NA	NC
NC	NA	AE19	PS_MIO19	NA	500	PSMIO	NA	NA	NC
64MB QSPI Flash	NA	AF15	PS_MIO2	NA	500	PSMIO	NA	+3V3_G	L_QSPI_D2
NC	NA	AD19	PS_MIO20	NA	500	PSMIO	NA	NA	NC
NC	NA	AC21	PS_MIO21	NA	500	PSMIO	NA	NA	NC
I2C	NA	AB20	PS_MIO22	NA	500	PSMIO	NA	NA	SCL
I2C	NA	AB18	PS_MIO23	NA	500	PSMIO	NA	NA	SDA
NC	NA	AB19	PS_MIO24	NA	500	PSMIO	NA	NA	NC
NC	NA	AB21	PS_MIO25	NA	500	PSMIO	NA	NA	NC
64MB QSPI Flash	NA	AH15	PS_MIO3	NA	500	PSMIO	NA	+3V3_G	L_QSPI_D3
64MB QSPI Flash	NA	AH16	PS_MIO4	NA	500	PSMIO	NA	+3V3_G	L_QSPI_D0
64MB QSPI Flash	NA	AD16	PS_MIO5	NA	500	PSMIO	NA	+3V3_G	L_QSPI_CSn
NC	NA	AF16	PS_MIO6	NA	500	PSMIO	NA	NA	NC
64MB QSPI Flash	NA	AH17	PS_MIO7	NA	500	PSMIO	NA	+3V3_G	U_QSPI_CSn
64MB QSPI Flash	NA	AF17	PS_MIO8	NA	500	PSMIO	NA	+3V3_G	U_QSPI_D0
64MB QSPI Flash	NA	AC16	PS_MIO9	NA	500	PSMIO	NA	+3V3_G	U_QSPI_D1
PS_IO	X2:122	L15	PS_MIO26	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:121	J15	PS_MIO27	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:124	K15	PS_MIO28	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:123	G16	PS_MIO29	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:128	F16	PS_MIO30	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:127	H16	PS_MIO31	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:130	J16	PS_MIO32	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:129	L16	PS_MIO33	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:132	L17	PS_MIO34	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:131	H17	PS_MIO35	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:134	K17	PS_MIO36	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:133	J17	PS_MIO37	NA	501	PSMIO	X2_MIO		+1V8
NC	NA	H18	PS_MIO38	NA	501	PSMIO	NA	NA	NC

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
NC	NA	H19	PS_MIO39	NA	501	PSMIO	NA	NA	NC
PS_IO	X2:159	K18	PS_MIO40	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:160	J19	PS_MIO41	NA	501	PSMIO	X2_MIO		+1V8
NC	NA	L18	PS_MIO42	NA	501	PSMIO	NA	NA	NC
NC	NA	K19	PS_MIO43	NA	501	PSMIO	NA	NA	NC
PS_IO	X2:157	J20	PS_MIO44	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:158	K20	PS_MIO45	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:152	L20	PS_MIO46	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:151	H21	PS_MIO47	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:156	J21	PS_MIO48	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:155	M18	PS_MIO49	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:149	M19	PS_MIO50	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:150	L21	PS_MIO51	NA	501	PSMIO	X2_MIO		+1V8
PS_IO	X2:146	G18	PS_MIO52	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:135	D16	PS_MIO53	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:144	F17	PS_MIO54	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:139	B16	PS_MIO55	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:142	C16	PS_MIO56	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:141	A16	PS_MIO57	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:140	F18	PS_MIO58	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:143	E17	PS_MIO59	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:136	C17	PS_MIO60	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:145	D17	PS_MIO61	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:148	A17	PS_MIO62	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:147	E18	PS_MIO63	NA	502	PSMIO	X2_MIO		+1V8
NC	NA	E19	PS_MIO64	NA	502	PSMIO	NA	NA	NC
NC	NA	A18	PS_MIO65	NA	502	PSMIO	NA	NA	NC
NC	NA	G19	PS_MIO66	NA	502	PSMIO	NA	NA	NC
NC	NA	B18	PS_MIO67	NA	502	PSMIO	NA	NA	NC
NC	NA	C18	PS_MIO68	NA	502	PSMIO	NA	NA	NC
NC	NA	D19	PS_MIO69	NA	502	PSMIO	NA	NA	NC
NC	NA	C19	PS_MIO70	NA	502	PSMIO	NA	NA	NC
NC	NA	B19	PS_MIO71	NA	502	PSMIO	NA	NA	NC
NC	NA	G20	PS_MIO72	NA	502	PSMIO	NA	NA	NC
NC	NA	G21	PS_MIO73	NA	502	PSMIO	NA	NA	NC
PS_IO	X2:162	D20	PS_MIO74	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:161	A19	PS_MIO75	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:164	B20	PS_MIO76	NA	502	PSMIO	X2_MIO		+1V8
PS_IO	X2:163	F20	PS_MIO77	NA	502	PSMIO	X2_MIO		+1V8
PS_DONE	NA	M21	PS_DONE	NA	503	PSCONFIG	NA		+3V3

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
NC	NA	P17	PS_ERROR_OUT	NA	503	PSCONFIG	NA	NA	NC
NC	NA	M20	PS_ERROR_STATUS	NA	503	PSCONFIG	NA	NA	NC
PS_INIT_B	NA	P21	PS_INIT_B	NA	503	PSCONFIG	NA		+3V3
JTAG	X2:117	R19	PS_JTAG_TCK	NA	503	PSCONFIG	X2		+3V3
JTAG	X2:119	R18	PS_JTAG_TDI	NA	503	PSCONFIG	X2		+3V3
JTAG	X2:120	T21	PS_JTAG_TDO	NA	503	PSCONFIG	X2		+3V3
JTAG	X2:118	N21	PS_JTAG_TMS	NA	503	PSCONFIG	X2		+3V3
MODE	NA	P19	PS_MODE0	NA	503	PSCONFIG	NA		+3V3
MODE	NA	P20	PS_MODE1	NA	503	PSCONFIG	NA		+3V3
MODE	NA	R20	PS_MODE2	NA	503	PSCONFIG	NA		+3V3
NC	NA	T20	PS_MODE3	NA	503	PSCONFIG	NA	NA	NC
PS_PADI	NA	N17	PS_PADI	NA	503	PSCONFIG	NA		+3V3
PS_PADO	NA	N18	PS_PADO	NA	503	PSCONFIG	NA		+3V3
PS_POR_B	NA	P16	PS_POR_B	NA	503	PSCONFIG	NA		+3V3
PS_PROG_B	NA	R17	PS_PROG_B	NA	503	PSCONFIG	NA		+3V3
PS_REF_CLK	NA	R16	PS_REF_CLK	NA	503	PSCONFIG	NA		+3V3
PS_SRST_B	NA	N19	PS_SRST_B	NA	503	PSCONFIG	NA		+3V3
PS_RAM	NA	W28	PS_DDR_A0	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A0 U301_A0 U302_A0 U303_A0
PS_RAM	NA	Y28	PS_DDR_A1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A1 U301_A1 U302_A1 U303_A1
PS_RAM	NA	AA25	PS_DDR_A10	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A10/AP U301_A10/AP U302_A10/AP U303_A10/AP
PS_RAM	NA	AA26	PS_DDR_A11	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A11 U301_A11 U302_A11 U303_A11
PS_RAM	NA	AB25	PS_DDR_A12	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A12/BC_n U301_A12/BC_n U302_A12/BC_n U303_A12/BC_n
PS_RAM	NA	AB26	PS_DDR_A13	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A13 U301_A13 U302_A13 U303_A13
PS_RAM	NA	AB24	PS_DDR_A14	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A14/WE_n U301_A14/WE_n U302_A14/WE_n U303_A14/WE_n
PS_RAM	NA	AC24	PS_DDR_A15	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A15/CAS_n U301_A15/CAS_n U302_A15/CAS_n U303_A15/CAS_n

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PS_RAM	NA	AC23	PS_DDR_A16	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A16/RAS_n U301_A16/RAS_n U302_A16/RAS_n U303_A16/RAS_n
PS_RAM	NA	AC22	PS_DDR_A17	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	AB28	PS_DDR_A2	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A2 U301_A2 U302_A2 U303_A2
PS_RAM	NA	AA28	PS_DDR_A3	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A3 U301_A3 U302_A3 U303_A3
PS_RAM	NA	Y27	PS_DDR_A4	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A4 U301_A4 U302_A4 U303_A4
PS_RAM	NA	AA27	PS_DDR_A5	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A5 U301_A5 U302_A5 U303_A5
PS_RAM	NA	Y22	PS_DDR_A6	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A6 U301_A6 U302_A6 U303_A6
PS_RAM	NA	AA23	PS_DDR_A7	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A7 U301_A7 U302_A7 U303_A7
PS_RAM	NA	AA22	PS_DDR_A8	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A8 U301_A8 U302_A8 U303_A8
PS_RAM	NA	AB23	PS_DDR_A9	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_A9 U301_A9 U302_A9 U303_A9
PS_RAM	NA	Y23	PS_DDR_ACT_N	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_ACT_n U301_ACT_n U302_ACT_n U303_ACT_n
PS_RAM	NA	U25	PS_DDR_ALERT_N	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_ALERT_n U301_ALERT_n U302_ALERT_n U303_ALERT_n
PS_RAM	NA	V23	PS_DDR_BA0	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_BA0 U301_BA0 U302_BA0 U303_BA0
PS_RAM	NA	W22	PS_DDR_BA1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_BA1 U301_BA1 U302_BA1 U303_BA1
PS_RAM	NA	W24	PS_DDR_BG0	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_BG0 U301_BG0 U302_BG0 U303_BG0
PS_RAM	NA	V22	PS_DDR_BG1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_BG1 U301_BG1 U302_BG1 U303_BG1
PS_RAM	NA	W25	PS_DDR_CK0	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_CK_t U301_CK_t U302_CK_t U303_CK_t
PS_RAM	NA	Y24	PS_DDR_CK1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PS_RAM	NA	V28	PS_DDR_CKE0	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_CKE U301_CKE U302_CKE U303_CKE
PS_RAM	NA	V27	PS_DDR_CKE1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	W26	PS_DDR_CK_N0	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_CK_c U301_CK_c U302_CK_c U303_CK_c
PS_RAM	NA	Y25	PS_DDR_CK_N1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	W27	PS_DDR_CS_N0	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_CS_n U301_CS_n U302_CS_n U303_CS_n
PS_RAM	NA	V26	PS_DDR_CS_N1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	AG20	PS_DDR_DM0	NA	504	PSDDR	NA	'+2V5_DRAM_VPP	U300_UDM
PS_RAM	NA	AE23	PS_DDR_DM1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_LDM
PS_RAM	NA	AE25	PS_DDR_DM2	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_UDM
PS_RAM	NA	AE28	PS_DDR_DM3	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_LDM
PS_RAM	NA	R23	PS_DDR_DM4	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_UDM
PS_RAM	NA	H23	PS_DDR_DM5	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_LDM
PS_RAM	NA	L27	PS_DDR_DM6	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_UDM
PS_RAM	NA	H26	PS_DDR_DM7	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_LDM
PS_RAM	NA	T26	PS_DDR_DM8	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	AD21	PS_DDR_DQ0	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_UDQ7
PS_RAM	NA	AE20	PS_DDR_DQ1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_UDQ2
PS_RAM	NA	AE22	PS_DDR_DQ10	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_LDQ6
PS_RAM	NA	AD22	PS_DDR_DQ11	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_LDQ7
PS_RAM	NA	AH23	PS_DDR_DQ12	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_LDQ0
PS_RAM	NA	AH24	PS_DDR_DQ13	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_LDQ1
PS_RAM	NA	AE24	PS_DDR_DQ14	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_LDQ5
PS_RAM	NA	AG24	PS_DDR_DQ15	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_LDQ3
PS_RAM	NA	AC26	PS_DDR_DQ16	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_UDQ7
PS_RAM	NA	AD26	PS_DDR_DQ17	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_UDQ5
PS_RAM	NA	AD25	PS_DDR_DQ18	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_UDQ2
PS_RAM	NA	AD24	PS_DDR_DQ19	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_UDQ0
PS_RAM	NA	AD20	PS_DDR_DQ2	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_UDQ0
PS_RAM	NA	AG26	PS_DDR_DQ20	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_UDQ3
PS_RAM	NA	AH25	PS_DDR_DQ21	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_UDQ6
PS_RAM	NA	AH26	PS_DDR_DQ22	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_UDQ1
PS_RAM	NA	AG25	PS_DDR_DQ23	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_UDQ4
PS_RAM	NA	AH27	PS_DDR_DQ24	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_LDQ1
PS_RAM	NA	AH28	PS_DDR_DQ25	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_LDQ0
PS_RAM	NA	AF28	PS_DDR_DQ26	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_LDQ3
PS_RAM	NA	AG28	PS_DDR_DQ27	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_LDQ2

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PS_RAM	NA	AC27	PS_DDR_DQ28	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_LDQ7
PS_RAM	NA	AD27	PS_DDR_DQ29	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_LDQ4
PS_RAM	NA	AF20	PS_DDR_DQ3	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_UDQ4
PS_RAM	NA	AD28	PS_DDR_DQ30	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_LDQ5
PS_RAM	NA	AC28	PS_DDR_DQ31	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_LDQ6
PS_RAM	NA	T22	PS_DDR_DQ32	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_UDQ4
PS_RAM	NA	R22	PS_DDR_DQ33	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_UDQ0
PS_RAM	NA	P22	PS_DDR_DQ34	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_UDQ7
PS_RAM	NA	N22	PS_DDR_DQ35	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_UDQ1
PS_RAM	NA	T23	PS_DDR_DQ36	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_UDQ2
PS_RAM	NA	P24	PS_DDR_DQ37	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_UDQ5
PS_RAM	NA	R24	PS_DDR_DQ38	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_UDQ6
PS_RAM	NA	N24	PS_DDR_DQ39	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_UDQ3
PS_RAM	NA	AH21	PS_DDR_DQ4	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_UDQ5
PS_RAM	NA	H24	PS_DDR_DQ40	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_LDQ2
PS_RAM	NA	J24	PS_DDR_DQ41	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_LDQ0
PS_RAM	NA	M24	PS_DDR_DQ42	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_LDQ4
PS_RAM	NA	K24	PS_DDR_DQ43	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_LDQ3
PS_RAM	NA	J22	PS_DDR_DQ44	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_LDQ7
PS_RAM	NA	H22	PS_DDR_DQ45	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_LDQ6
PS_RAM	NA	K22	PS_DDR_DQ46	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_LDQ5
PS_RAM	NA	L22	PS_DDR_DQ47	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_LDQ1
PS_RAM	NA	M25	PS_DDR_DQ48	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_UDQ1
PS_RAM	NA	M26	PS_DDR_DQ49	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_UDQ3
PS_RAM	NA	AH20	PS_DDR_DQ5	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_UDQ1
PS_RAM	NA	L25	PS_DDR_DQ50	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_UDQ5
PS_RAM	NA	L26	PS_DDR_DQ51	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_UDQ7
PS_RAM	NA	K28	PS_DDR_DQ52	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_UDQ6
PS_RAM	NA	L28	PS_DDR_DQ53	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_UDQ2
PS_RAM	NA	M28	PS_DDR_DQ54	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_UDQ4
PS_RAM	NA	N28	PS_DDR_DQ55	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_UDQ0
PS_RAM	NA	J28	PS_DDR_DQ56	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_LDQ4
PS_RAM	NA	K27	PS_DDR_DQ57	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_LDQ0
PS_RAM	NA	H28	PS_DDR_DQ58	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_LDQ3
PS_RAM	NA	H27	PS_DDR_DQ59	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_LDQ2
PS_RAM	NA	AH19	PS_DDR_DQ6	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_UDQ3
PS_RAM	NA	G26	PS_DDR_DQ60	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_LDQ6
PS_RAM	NA	G25	PS_DDR_DQ61	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_LDQ7
PS_RAM	NA	K25	PS_DDR_DQ62	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_LDQ1
PS_RAM	NA	J25	PS_DDR_DQ63	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_LDQ5

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PS_RAM	NA	T28	PS_DDR_DQ64	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	R28	PS_DDR_DQ65	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	P28	PS_DDR_DQ66	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	P27	PS_DDR_DQ67	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	P26	PS_DDR_DQ68	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	R25	PS_DDR_DQ69	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	AG19	PS_DDR_DQ7	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_UDQ6
PS_RAM	NA	P25	PS_DDR_DQ70	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	T25	PS_DDR_DQ71	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	AF22	PS_DDR_DQ8	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_LDQ2
PS_RAM	NA	AH22	PS_DDR_DQ9	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_LDQ4
PS_RAM	NA	AG21	PS_DDR_DQS_N0	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_UDQS_c
PS_RAM	NA	AG23	PS_DDR_DQS_N1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_LDQS_c
PS_RAM	NA	AF26	PS_DDR_DQS_N2	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_UDQS_c
PS_RAM	NA	AF27	PS_DDR_DQS_N3	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_LDQS_c
PS_RAM	NA	M23	PS_DDR_DQS_N4	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_UDQS_c
PS_RAM	NA	K23	PS_DDR_DQS_N5	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_LDQS_c
PS_RAM	NA	N27	PS_DDR_DQS_N6	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_UDQS_c
PS_RAM	NA	J27	PS_DDR_DQS_N7	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_LDQS_c
PS_RAM	NA	T27	PS_DDR_DQS_N8	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	AF21	PS_DDR_DQS_P0	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_UDQS_t
PS_RAM	NA	AF23	PS_DDR_DQS_P1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_LDQS_t
PS_RAM	NA	AF25	PS_DDR_DQS_P2	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_UDQS_t
PS_RAM	NA	AE27	PS_DDR_DQS_P3	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U301_LDQS_t
PS_RAM	NA	N23	PS_DDR_DQS_P4	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_UDQS_t
PS_RAM	NA	L23	PS_DDR_DQS_P5	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U303_LDQS_t
PS_RAM	NA	N26	PS_DDR_DQS_P6	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_UDQS_t
PS_RAM	NA	J26	PS_DDR_DQS_P7	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U302_LDQS_t
PS_RAM	NA	R27	PS_DDR_DQS_P8	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	U28	PS_DDR_ODT0	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_ODT U301_ODT U302_ODT U303_ODT
PS_RAM	NA	U26	PS_DDR_ODT1	NA	504	PSDDR	NA	+2V5_DRAM_VPP	NC
PS_RAM	NA	V24	PS_DDR_PARITY	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_PAR U301_PAR U302_PAR U303_PAR
PS_RAM	NA	U23	PS_DDR_RAM_RST_N	NA	504	PSDDR	NA	+2V5_DRAM_VPP	U300_RESET_n U301_RESET_n U302_RESET_n U303_RESET_n
PS_RAM	NA	U24	PS_DDR_ZQ	NA	504	PSDDR	NA	GND	NC
MGT	X600:28	F28	PS_MGTRRXN0_505	NA	505	PSGTR	NA		

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
MGT	X600:22	D28	PS_MGTRRXN1_505	NA	505	PSGTR	NA		
MGT	X600:16	B28	PS_MGTRRXN2_505	NA	505	PSGTR	NA		
MGT	X600:10	A26	PS_MGTRRXN3_505	NA	505	PSGTR	NA		
MGT	X600:26	F27	PS_MGTRRXP0_505	NA	505	PSGTR	NA		
MGT	X600:20	D27	PS_MGTRRXP1_505	NA	505	PSGTR	NA		
MGT	X600:14	B27	PS_MGTRRXP2_505	NA	505	PSGTR	NA		
MGT	X600:8	A25	PS_MGTRRXP3_505	NA	505	PSGTR	NA		
MGT	X600:27	E26	PS_MGTRTXN0_505	NA	505	PSGTR	NA		
MGT	X600:21	D24	PS_MGTRTXN1_505	NA	505	PSGTR	NA		
MGT	X600:15	C26	PS_MGTRTXN2_505	NA	505	PSGTR	NA		
MGT	X600:9	B24	PS_MGTRTXN3_505	NA	505	PSGTR	NA		
MGT	X600:25	E25	PS_MGTRTXP0_505	NA	505	PSGTR	NA		
MGT	X600:19	D23	PS_MGTRTXP1_505	NA	505	PSGTR	NA		
MGT	X600:13	C25	PS_MGTRTXP2_505	NA	505	PSGTR	NA		
MGT	X600:7	B23	PS_MGTRTXP3_505	NA	505	PSGTR	NA		
MGT	NA	F24	PS_MGTREFCLK0N_505	NA	505	PSGTR	NA		
MGT	NA	F23	PS_MGTREFCLK0P_505	NA	505	PSGTR	NA		
MGT	NA	E22	PS_MGTREFCLK1N_505	NA	505	PSGTR	NA		
MGT	NA	E21	PS_MGTREFCLK1P_505	NA	505	PSGTR	NA		
MGT	NA	C22	PS_MGTREFCLK2N_505	NA	505	PSGTR	NA		
MGT	NA	C21	PS_MGTREFCLK2P_505	NA	505	PSGTR	NA		
MGT	NA	A22	PS_MGTREFCLK3N_505	NA	505	PSGTR	NA		
MGT	NA	A21	PS_MGTREFCLK3P_505	NA	505	PSGTR	NA		
MGT	NA	F22	PS_MGTRREF_505	NA	NA	NA	NA	GND	
VCCO	X1:83	AA14	VCCO	NA	XCZU5/4 : 44 XCZU3/2 : 24	NA	X1_2	VIO_X1_2	USER DEF
VCCO	X1:83	AD13	VCCO	NA	XCZU5/4 : 44 XCZU3/2 : 24	NA	X1_2	VIO_X1_2	USER DEF
VCCO	X1:30	B12	VCCO	NA	XCZU5/4 : 45 XCZU3/2 : 25	NA	X1_1	VIO_X1_1	USER DEF
VCCO	X1:30	E11	VCCO	NA	XCZU5/4 : 45 XCZU3/2 : 25	NA	X1_1	VIO_X1_1	USER DEF
VCCO	X1:29	C15	VCCO	NA	XCZU5/4 : 46 XCZU3/2 : 26	NA	X1_1	VIO_X1_1	USER DEF
VCCO	X1:29	F14	VCCO	NA	XCZU5/4 : 46 XCZU3/2 : 26	NA	X1_1	VIO_X1_1	USER DEF
VCCO	X1:84	AC10	VCCO	NA	XCZU5/4 : 43 XCZU3/2 : 44	NA	X1_2	VIO_X1_2	USER DEF
VCCO	X1:84	AG12	VCCO	NA	XCZU5/4 : 43 XCZU3/2 : 44	NA	X1_2	VIO_X1_2	USER DEF
VCCO_64	NA	AC5	VCCO_64	NA	64	NA	NA	VCC_DDR	+1V2
VCCO_64	NA	AD8	VCCO_64	NA	64	NA	NA	VCC_DDR	+1V2
VCCO_64	NA	AG7	VCCO_64	NA	64	NA	NA	VCC_DDR	+1V2
VCCO_65	NA	H5	VCCO_65	NA	65	NA	NA		T804_VOUT

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
VCCO_65	NA	J3	VCCO_65	NA	65	NA	NA		T804_VOUT
VCCO_65	NA	L4	VCCO_65	NA	65	NA	NA		T804_VOUT
VCCO_66	NA	B7	VCCO_66	NA	66	NA	NA		T805_VOUT
VCCO_66	NA	D3	VCCO_66	NA	66	NA	NA		T805_VOUT
VCCO_66	NA	E6	VCCO_66	NA	66	NA	NA		T805_VOUT
VCCO_PSIO0_500	X1:+3V3_G X2:+3V3_G	AB17	VCCO_PSIO0_500	NA	500	NA	NA	NA	+3V3
VCCO_PSIO0_500	X1:+3V3_G X2:+3V3_G	AE16	VCCO_PSIO0_500	NA	500	NA	NA	NA	+3V3
VCCO_PSIO0_500	X1:+3V3_G X2:+3V3_G	AG17	VCCO_PSIO0_500	NA	500	NA	NA	NA	+3V3
VCCO_PSIO1_501	NA	H20	VCCO_PSIO1_501	NA	501	NA	NA	+1V8_VCC_AUX	+1V8
VCCO_PSIO1_501	NA	L19	VCCO_PSIO1_501	NA	501	NA	NA	+1V8_VCC_AUX	+1V8
VCCO_PSIO2_502	NA	D18	VCCO_PSIO2_502	NA	502	NA	NA	+1V8_VCC_AUX	+1V8
VCCO_PSIO2_502	NA	G17	VCCO_PSIO2_502	NA	502	NA	NA	+1V8_VCC_AUX	+1V8
VCCO_PSIO3_503	X1:+3V3_G X2:+3V3_G	M17	VCCO_PSIO3_503	NA	503	NA	NA	NA	+3V3
VCCO_PSIO3_503	X1:+3V3_G X2:+3V3_G	P18	VCCO_PSIO3_503	NA	503	NA	NA	NA	+3V3
VCCO_PSDDR_504	NA	AB22	VCCO_PSDDR_504	NA	504	NA	NA	VCC_DDR	+1V2
VCCO_PSDDR_504	NA	AD23	VCCO_PSDDR_504	NA	504	NA	NA	VCC_DDR	+1V2
VCCO_PSDDR_504	NA	AF24	VCCO_PSDDR_504	NA	504	NA	NA	VCC_DDR	+1V2
VCCO_PSDDR_504	NA	P23	VCCO_PSDDR_504	NA	504	NA	NA	VCC_DDR	+1V2
VCCO_PSDDR_504	NA	T24	VCCO_PSDDR_504	NA	504	NA	NA	VCC_DDR	+1V2
VCCO_PSDDR_504	NA	V25	VCCO_PSDDR_504	NA	504	NA	NA	VCC_DDR	+1V2
VCCO_PSDDR_504	NA	Y26	VCCO_PSDDR_504	NA	504	NA	NA	VCC_DDR	+1V2
GND	X1/2:GND	A20	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	A24	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	A27	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	A28	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AA1	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AA19	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AA2	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AA24	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AA3	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AA4	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AA5	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AA6	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AA9	GND	NA	NA	NA	NA	GND	

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
GND	X1/2:GND	AB12	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AB27	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AC15	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AC20	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AC25	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AD18	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AD3	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AE1	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AE11	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AE21	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AE26	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AE6	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AF14	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AF19	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AF4	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AF9	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AG2	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AG22	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AG27	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	AH5	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	B17	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	B2	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	B21	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	B25	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	B26	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	C10	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	C20	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	C24	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	C27	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	C28	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	C5	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	D13	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	D21	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	D26	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	D8	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	E16	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	E20	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	E24	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	E27	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	E28	GND	NA	NA	NA	NA	GND	

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
GND	X1/2:GND	F19	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	F21	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	F25	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	F26	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	F4	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	F9	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	G12	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	G2	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	G22	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	G23	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	G24	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	G27	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	G28	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	G7	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	H10	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	H15	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	H25	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	J13	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	J18	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	J23	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	J8	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	K11	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	K16	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	K21	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	K26	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	K6	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	L24	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	L9	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	M1	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	M2	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	M22	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	M27	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	M3	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	M4	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	M5	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	M7	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	N10	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	N12	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	N14	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	N20	GND	NA	NA	NA	NA	GND	

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
GND	X1/2:GND	N25	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	N5	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	P11	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	P3	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	P5	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	P8	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	R1	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	R15	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	R2	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	R21	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	R26	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	R5	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	T10	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	T14	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	T19	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	T3	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	T5	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	T9	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	U1	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	U11	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	U17	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	U2	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	U22	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	U27	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	U6	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	V13	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	V15	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	V3	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	V7	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	W1	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	W18	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	W2	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	W23	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	W6	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	Y11	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	Y16	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	Y3	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	Y7	GND	NA	NA	NA	NA	GND	
GND	X1/2:GND	W20	GND_PSADC	NA	NA	NA	NA	GND	
MGT_PWR	NA	B22	PS_MGTRAVCC	NA	NA	NA	NA	+0V85_PSMGT_AVCC	+0V85

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
MGT_PWR	NA	D22	PS_MGTRAVCC	NA	NA	NA	NA	+0V85_PSMGT_AVCC	+0V85
MGT_PWR	NA	A23	PS_MGTRAVTT	NA	NA	NA	NA	+1V8_PSMGT_AVTT	+1V8
MGT_PWR	NA	C23	PS_MGTRAVTT	NA	NA	NA	NA	+1V8_PSMGT_AVTT	+1V8
MGT_PWR	NA	D25	PS_MGTRAVTT	NA	NA	NA	NA	+1V8_PSMGT_AVTT	+1V8
MGT_PWR	NA	E23	PS_MGTRAVTT	NA	NA	NA	NA	+1V8_PSMGT_AVTT	+1V8
VCCAUX	NA	M16	VCCAUX	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8
VCCAUX	NA	N16	VCCAUX	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8
VCCAUX	NA	M13	VCCAUX	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8
VCCAUX	NA	M14	VCCAUX	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8
VCCAUX	NA	M15	VCCAUX	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8
VCCBRAM	NA	L11	VCCBRAM	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCCBRAM	NA	L12	VCCBRAM	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCCBRAM	NA	M11	VCCBRAM	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCCBRAM	NA	M12	VCCBRAM	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCCINT	NA	N11	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	N13	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	N15	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	P10	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	P14	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	P15	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	R10	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	R11	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	R14	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	T11	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	T15	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	U10	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	U14	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	U15	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	V10	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	V11	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	V12	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT	NA	V14	VCCINT	NA	NA	NA	NA	+VCC_INT	+VCC_INT
VCCINT_IO	NA	K10	VCCINT_IO	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCCINT_IO	NA	L10	VCCINT_IO	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCCINT_IO	NA	M10	VCCINT_IO	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCCINT_IO	NA	M9	VCCINT_IO	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSADC	NA	Y20	VCC_PSADC	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8
VCC_PSAUX	NA	U19	VCC_PSAUX	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8
VCC_PSAUX	NA	U20	VCC_PSAUX	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8
VCC_PSAUX	NA	V19	VCC_PSAUX	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
VCC_PSAUX	NA	W19	VCC_PSAUX	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8
VCC_PSBATT	X2:126	Y18	VCC_PSBATT	NA	NA	NA	X2_VBATT_IN	X2_VBATT_IN	+1.2V -> +1.5V
VCC_PSDDR_PLL	NA	U16	VCC_PSDDR_PLL	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8
VCC_PSDDR_PLL	NA	U18	VCC_PSDDR_PLL	NA	NA	NA	NA	+1V8_VCC_AUX	+1V8
VCC_PSINTFP	NA	AA15	VCC_PSINTFP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTFP	NA	AA16	VCC_PSINTFP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTFP	NA	AA17	VCC_PSINTFP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTFP	NA	AA18	VCC_PSINTFP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTFP	NA	AB16	VCC_PSINTFP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTFP	NA	Y15	VCC_PSINTFP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTFP	NA	Y17	VCC_PSINTFP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTFP_DDR	NA	AA20	VCC_PSINTFP_DDR	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTFP_DDR	NA	AA21	VCC_PSINTFP_DDR	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTFP_DDR	NA	Y19	VCC_PSINTFP_DDR	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTLP	NA	V16	VCC_PSINTLP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTLP	NA	V17	VCC_PSINTLP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTLP	NA	V18	VCC_PSINTLP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTLP	NA	W15	VCC_PSINTLP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTLP	NA	W16	VCC_PSINTLP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSINTLP	NA	W17	VCC_PSINTLP	NA	NA	NA	NA	+VCC_INT_IO	+VCC_INT_IO
VCC_PSPLL	NA	T16	VCC_PSPLL	NA	NA	NA	NA	+1V2_MGT_AVTT	+1V2
VCC_PSPLL	NA	T17	VCC_PSPLL	NA	NA	NA	NA	+1V2_MGT_AVTT	+1V2
VCC_PSPLL	NA	T18	VCC_PSPLL	NA	NA	NA	NA	+1V2_MGT_AVTT	+1V2
EV: VCCINT_VCU EG/CG : RSVD_GND	NA	U21	EV: VCCINT_VCU EG/CG : RSVD_GND	NA	NA	NA	NA	EV : +0V9_INT_VCU EG/CG : GND	EV : +0V9 EG/CG : GND
EV: VCCINT_VCU EG/CG : RSVD_GND	NA	V20	EV: VCCINT_VCU EG/CG : RSVD_GND	NA	NA	NA	NA	EV : +0V9_INT_VCU EG/CG : GND	EV : +0V9 EG/CG : GND
EV: VCCINT_VCU EG/CG : RSVD_GND	NA	V21	EV: VCCINT_VCU EG/CG : RSVD_GND	NA	NA	NA	NA	EV : +0V9_INT_VCU EG/CG : GND	EV : +0V9 EG/CG : GND
EV: VCCINT_VCU EG/CG : RSVD_GND	NA	W21	EV: VCCINT_VCU EG/CG : RSVD_GND	NA	NA	NA	NA	EV : +0V9_INT_VCU EG/CG : GND	EV : +0V9 EG/CG : GND
EV: VCCINT_VCU EG/CG : RSVD_GND	NA	Y21	EV: VCCINT_VCU EG/CG : RSVD_GND	NA	NA	NA	NA	EV : +0V9_INT_VCU EG/CG : GND	EV : +0V9 EG/CG : GND
XCZU5/4 : MGTAVTTRCAL_R XCZU3/2 : NC	NA	N1	XCZU5/4 : MGTAVTTRCAL_R XCZU3/2 : NC	NA	NA	NA	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTRREF_R XCZU3/2 : NC	NA	N2	XCZU5/4 : MGTRREF_R XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:161 (XCZU5/4)	N3	XCZU5/4 : MGTHTXN3_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:159 (XCZU5/4)	N4	XCZU5/4 : MGTHTXP3_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
XCZU5/4 : MGTH XCZU3/2 : NC	X1:162 (XCZU5/4)	P1	XCZU5/4 : MGTHRXN3_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:160 (XCZU5/4)	P2	XCZU5/4 : MGTHRXP3_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTAVTT_R XCZU3/2 : NC	NA	P4	XCZU5/4 : MGTAVTT_R XCZU3/2 : NC	NA	NA	NA	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:155 (XCZU5/4)	R3	XCZU5/4 : MGTHTXN2_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:153 (XCZU5/4)	R4	XCZU5/4 : MGTHTXP2_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:156 (XCZU5/4)	T1	XCZU5/4 : MGTHRXN2_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:154 (XCZU5/4)	T2	XCZU5/4 : MGTHRXP2_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTAVTT_R XCZU3/2 : NC	NA	T4	XCZU5/4 : MGTAVTT_R XCZU3/2 : NC	NA	NA	NA	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:149 (XCZU5/4)	U3	XCZU5/4 : MGTHTXN1_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:147 (XCZU5/4)	U4	XCZU5/4 : MGTHTXP1_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTVCCAUX_R XCZU3/2 : NC	NA	U5	XCZU5/4 : MGTVCCAUX_R XCZU3/2 : NC	NA	NA	NA	NA	+1V8_VCC_AUX (XCZU5/4)	+1V8
XCZU5/4 : MGTH XCZU3/2 : NC	X1:150 (XCZU5/4)	V1	XCZU5/4 : MGTHRXN1_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:148 (XCZU5/4)	V2	XCZU5/4 : MGTHRXP1_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTAVCC_R XCZU3/2 : NC	NA	V4	XCZU5/4 : MGTAVCC_R XCZU3/2 : NC	NA	NA	NA	NA	+0V9_MGT_AVCC (XCZU5/4)	+0V9
XCZU5/4 : MGTREFCLK1N _224 XCZU3/2 : NC	NA	V5	XCZU5/4 : MGTREFCLK1N_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTREFCLK1P_ 224 XCZU3/2 : NC	NA	V6	XCZU5/4 : MGTREFCLK1P_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:143 (XCZU5/4)	W3	XCZU5/4 : MGTHTXN0_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:141 (XCZU5/4)	W4	XCZU5/4 : MGTHTXP0_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTVCCAUX_R XCZU3/2 : NC	NA	W5	XCZU5/4 : MGTVCCAUX_R XCZU3/2 : NC	NA	NA	NA	NA	+1V8_VCC_AUX (XCZU5/4)	+1V8
XCZU5/4 : MGTH XCZU3/2 : NC	X1:144 (XCZU5/4)	Y1	XCZU5/4 : MGTHRXN0_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTH XCZU3/2 : NC	X1:142 (XCZU5/4)	Y2	XCZU5/4 : MGTHRXP0_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTAVCC_R XCZU3/2 : NC	NA	Y4	XCZU5/4 : MGTAVCC_R XCZU3/2 : NC	NA	NA	NA	NA	+0V9_MGT_AVCC (XCZU5/4)	+0V9
XCZU5/4 : MGTREFCLK0N _224 XCZU3/2 : NC	NA	Y5	XCZU5/4 : MGTREFCLK0N_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
XCZU5/4 : MGTREFCLK0P_ 224 XCZU3/2 : NC	NA	Y6	XCZU5/4 : MGTREFCLK0P_224 XCZU3/2 : NC	NA	224 (XCZU5/4)	GTH (XCZU5/4)	NA	+1V2_MGT_AVTT (XCZU5/4)	+1V2
MGT_CLK.0_P	X1:135	NA	NA	NA	NA	NA	NA		

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
MGT_CLK.0_N	X1:137	NA	NA	NA	NA	NA	NA		
+3V3_G	X1:168	NA	+3V3_G	NA	NA	NA	NA	+3V3_G	+3V3
MGT_CLK.1_P	X1:136	NA	NA	NA	NA	NA	NA		
MGT_CLK.1_N	X1:138	NA	NA	NA	NA	NA	NA		
+3V3_G	X1:1	NA	+3V3_G	NA	NA	NA	NA	+3V3_G	+3V3
+3V3_G	X1:2	NA	+3V3_G	NA	NA	NA	NA	+3V3_G	+3V3
GND	X1:27	NA	GND	NA	NA	NA	X1_1	GND	
GND	X1:28	NA	GND	NA	NA	NA	X1_1	GND	
GND	X1:55	NA	GND	NA	NA	NA	X1_1	GND	
GND	X1:56	NA	GND	NA	NA	NA	X1_1	GND	
GND	X1:81	NA	GND	NA	NA	NA	X1_2	GND	
GND	X1:82	NA	GND	NA	NA	NA	X1_2	GND	
GND	X1:109	NA	GND	NA	NA	NA	X1_2	GND	
GND	X1:110	NA	GND	NA	NA	NA	X1_2	GND	
NC	X1:111	NA	NA	NA	NA	NA	NA		
NC	X1:112	NA	NA	NA	NA	NA	NA		
NC	X1:113	NA	NA	NA	NA	NA	NA		
NC	X1:114	NA	NA	NA	NA	NA	NA		
GND	X1:115	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:116	NA	GND	NA	NA	NA	MGT	GND	
NC	X1:117	NA	NA	NA	NA	NA	NA		
NC	X1:118	NA	NA	NA	NA	NA	NA		
NC	X1:119	NA	NA	NA	NA	NA	NA		
NC	X1:120	NA	NA	NA	NA	NA	NA		
GND	X1:121	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:122	NA	GND	NA	NA	NA	MGT	GND	
NC	X1:123	NA	NA	NA	NA	NA	NA		
NC	X1:124	NA	NA	NA	NA	NA	NA		
NC	X1:125	NA	NA	NA	NA	NA	NA		
NC	X1:126	NA	NA	NA	NA	NA	NA		
GND	X1:127	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:128	NA	GND	NA	NA	NA	MGT	GND	
NC	X1:129	NA	NA	NA	NA	NA	NA		
NC	X1:130	NA	NA	NA	NA	NA	NA		
NC	X1:131	NA	NA	NA	NA	NA	NA		
NC	X1:132	NA	NA	NA	NA	NA	NA		
GND	X1:133	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:134	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:139	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:140	NA	GND	NA	NA	NA	MGT	GND	

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
GND	X1:145	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:146	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:151	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:152	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:157	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:158	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:163	NA	GND	NA	NA	NA	MGT	GND	
GND	X1:164	NA	GND	NA	NA	NA	MGT	GND	
+3V3_G	X1:165	NA	+3V3_G	NA	NA	NA	NA	+3V3_G	+3V3
+3V3_G	X1:166	NA	+3V3_G	NA	NA	NA	NA	+3V3_G	+3V3
+3V3_G	X1:167	NA	+3V3_G	NA	NA	NA	NA	+3V3_G	+3V3
+3V3_G	X1:168	NA	+3V3_G	NA	NA	NA	NA	+3V3_G	+3V3

Compliance

All KRM modules are ROHSII and REACH compliant. For further details, customers may request the current declaration of conformity by emailing office@knowres.ch.
All KRM Modules are manufactured with UL94V-0 flammability rated PCBs with an IPC Class2 quality rating.

Electrical Specification

ESD

KRM Modules are sensitive to electrostatic discharge and must be handled with proper ESD precautions.

Absolute Maximum Ratings[i]

Symbol	Description	Min	Max
POWER_IN	Global power in	-0V5	3V6
VCCO_45/6 43/4	HD Bank I/O power supply	-0V5	3V6
VCCO_65/66	HP Bank I/O power supply	-0V5	2V0
V_BATT_IN	Encryption key storage supply	-0V5	2V0
PS_IO	MIO Bank I/O signal levels	-0V5	2V0
PL_IO_HP	HD Bank I/O signal levels	-0V5	2V0
PL_IO_HR	HR Bank I/O signal levels	-0V5	3V6

Recommended Operating conditions

Symbol	Description	Min	Typ	Max
POWER_IN	Global power in	3V2	3V3	3V4
VCCO_45/6 43/4	HD Bank I/O power supply	3V2	3V3	3V4
VCCO_65/66	HP Bank I/O power supply	1V7	1V8	1V89
V_BATT_IN	Encryption key storage supply	1V0	--	1V89
PS_IO	MIO Bank I/O signal levels[ii]	-0V2	--	VCCO + 0V2
PL_IO_HP	HD Bank I/O signal levels	-0V2	--	VCCO + 0V2
PL_IO_HR	HR Bank I/O signal levels	-0V2	--	VCCO + 0V2

[i] Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied.
Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect module reliability
[ii] For I/O operation, refer to the Xilinx *Ultrascale architecture SelectIO Resources User Guide* (UG571) or the Xilinx *Zynq-UltraScale+ Device Technical Reference Manual* (UG1085).

Thermal specification

Absolute Maximum Ratings[iii]

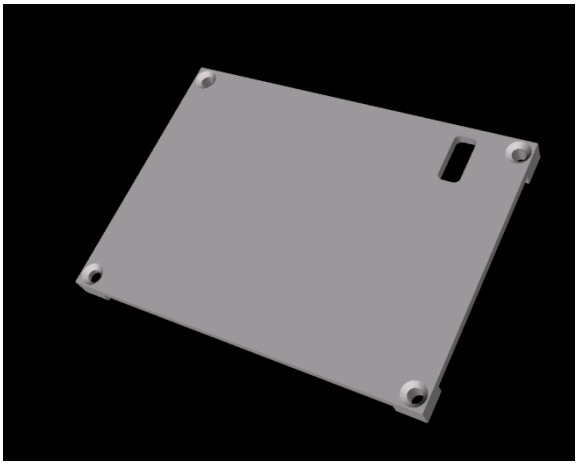
Symbol	Description	Min	Max
Delta T	Max temperature change per second while operating	--	+/-1°C/sec
TSTG	Storage temperature ambient un-powered	-40°C	+125°C

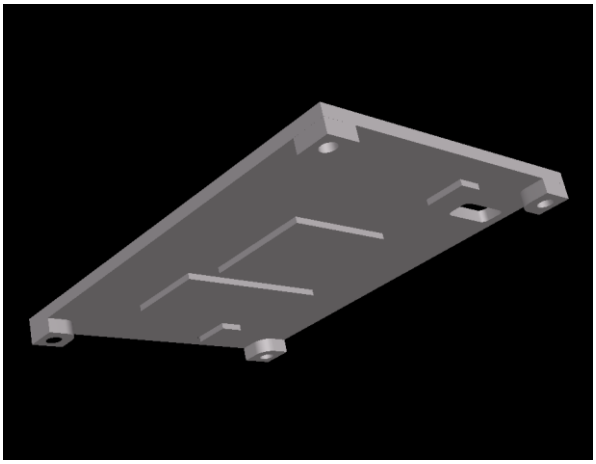
Recommended Operating Conditions

Symbol	Description	Min	Typ	Max
Tj E	Operating Junction temperature of FPGA for extended grade[iv]	0°C	--	+85°C
Tj I	Operating Junction temperature of FPGA for industrial grade	-40°C	--	+85°C
Delta T	Allowed temperature change per second while operating	--	--	+/-0.5°C/sec

Heat Management

The thermal load of the Module depends greatly on the user application, and is driven by clock speed, toggle rate, logic utilization, active peripherals and CPU utilization. The user must ensure that the generated heat is adequately removed from the module so that the Recommended Operating Conditions are not exceeded.
In order to ensure a consistent thermal interface across all KRM-3xxx module variants, KR offers a module-specific heat-spreader plate. The plate is simply an adapter and is not designed as a standalone cooling solution. In some low power applications of the smaller module variants, the spreader plate may be sufficient as a standalone solution.





[iii] Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied.
[iv] The upper operating temperature of the extended temperature module is limited by the maximum temperature of the industrial grade DDR4 RAM components with a Tj MAX of +85°C. Inquire for other options.

Module configurations

The KRM3-ZUxx Modules can be purchased in a multitude of configurations as shown in the table below. Option codes shown in black are valid options for this family, not all valid options may be combined (for example boot option set to on-board QSPI, but no Flash populated is invalid)
Blue option codes may become future options of this module family.

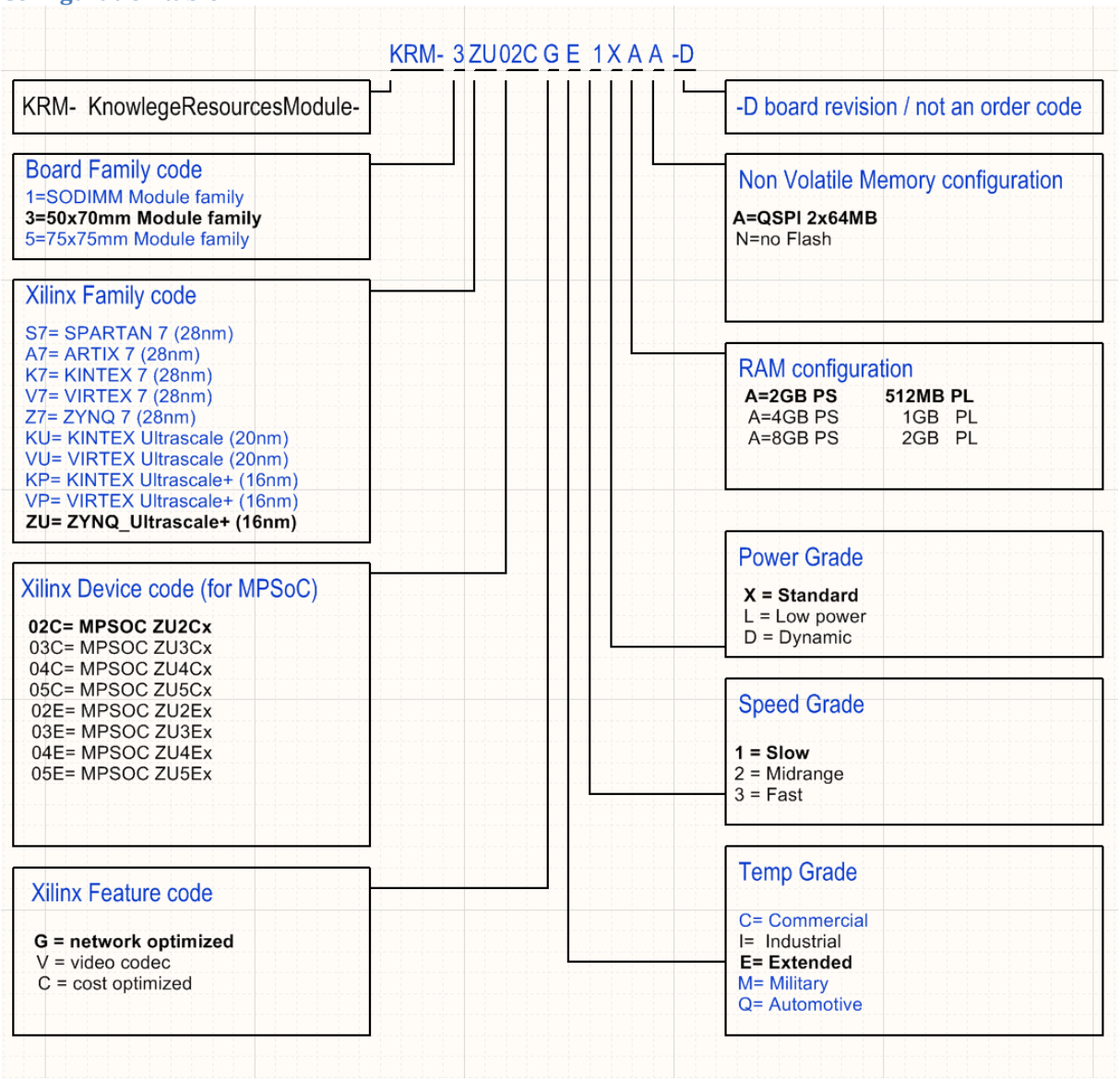
Standard Low quantity configuration

The standard assembly variant, which is orderable as samples, is as follows:

KRM-3ZU02CGE1XAA-D

50x70mm module family, with a Zynq Ultrascale+ ZU2 Extended temperature range, 2GB of PS Ram, 512MB of PL RAM, speed grade1 and dual QSPI populated.

Configuration table



Module Identification

Xilinx is no longer labeling its parts with speed grade and temperature grade information. The KRM PCB is also only labelled with the generic family code and contains no clear text information about its configuration. This makes it all but impossible to identify the modules detailed configuration.

All modules can be identified by scanning the QR code label that is mounted on the PS DDR memory components. The QR code contains a unique URL that will query the database of the KR test system and will produce a PDF document that contains information about the factory configuration of the module and test sequence the module passed after production.

Errata

No known errata at the time of writing