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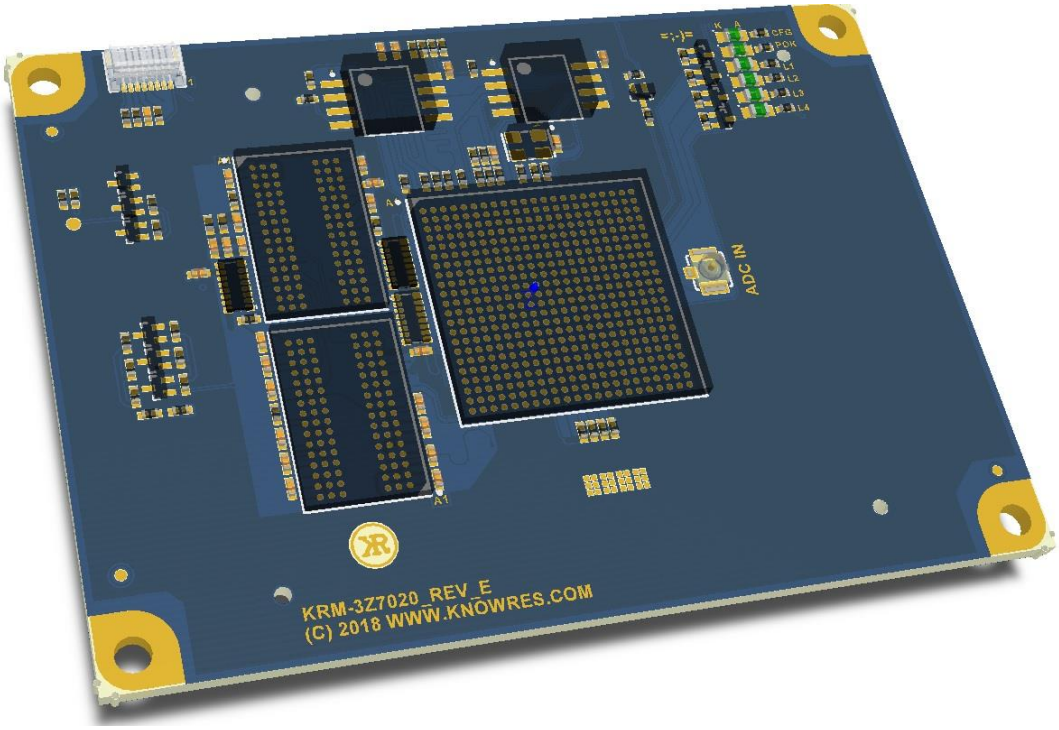
KRM-3Z7020

Data sheet Rev 1.9



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Revision History

Date	Document revision	HW revision	Changes
Aug.23rd 2013	0.1	REV A	First draft
Sept. 29th 2013	1.0	REV A	First public release
Oct. 12th 2013	1.1	REV B	Updated HW rev to production version
Feb. 2014	1.2	REV B	X1 and X2 PIN Mapping changes. Double entry X2:31, X2:32 corrected to X2:33, X2:34 > GND
March 17th 2014	1.3	REV B	-Added subchapter on I/O power sequencing -Changed minimum I/O voltage spec from 1V2 to 1V35
March 25th 2014	1.4	REV B	Disclaimer and board to board dimension added
October 27th 2014	1.5	REV B	Minor corrections
February 15th 2016	1.6	REV B	Updated nomenclature Configuration table added Hirose connector pinning clarification added Updated connector schematic with template
November 7th 2019	1.7	REV E/F	Added Board Management Controller information Updated Acronyms part Updated Mode pins part Updated Reset part with HW_RESET_IN Added VCCBATT_0 part Updated Connector Schematic with HW_RESET_IN and V_BATT_IN pins Updated Pin Mapping part with HW_RESET_IN and V_BATT_IN Updated illustration in title part Updated Board Dimensions
November 29th 2019	1.8	REV_E/F	Removed obsolete web links Generalized Xilinx SoC Type with reference to Module configurations Updated reset recommendations Added reference to QR code for module identification Typographical edits
February 13rd 2020	1.9	REV_E/F	Corrected hyperlinks

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Assumptions

The reader is familiar with Xilinx FPGA and SoC components and the related terminology in common use.

Acronyms

FU:	Future Use
KR:	Knowledge Resources GmbH
MIG:	Memory Interface Generator, a tool of Xilinx to easily implement a DDR3 controller
NA:	Not Applicable
OC:	On Chip
PL:	Programmable Logic
PS:	Processing Subsystem
SoC:	System on Chip
BMC:	Board Management Controller

Reference documents

ZYNQ all programmable SoC, Xilinx, www.xilinx.com

Support

KR will provide free of charge to qualified customers:

-Schematic and PCB libraries with Module and carrier board design components (Altium)
-3D STEP models of the module and heat spreader plate
-LINUX BSP and LINUX port (Plug and Boot ready)
-Reference schematics of the evaluation boards (Altium native and PDF)
-Vivado Project scripts to accelerate design starts

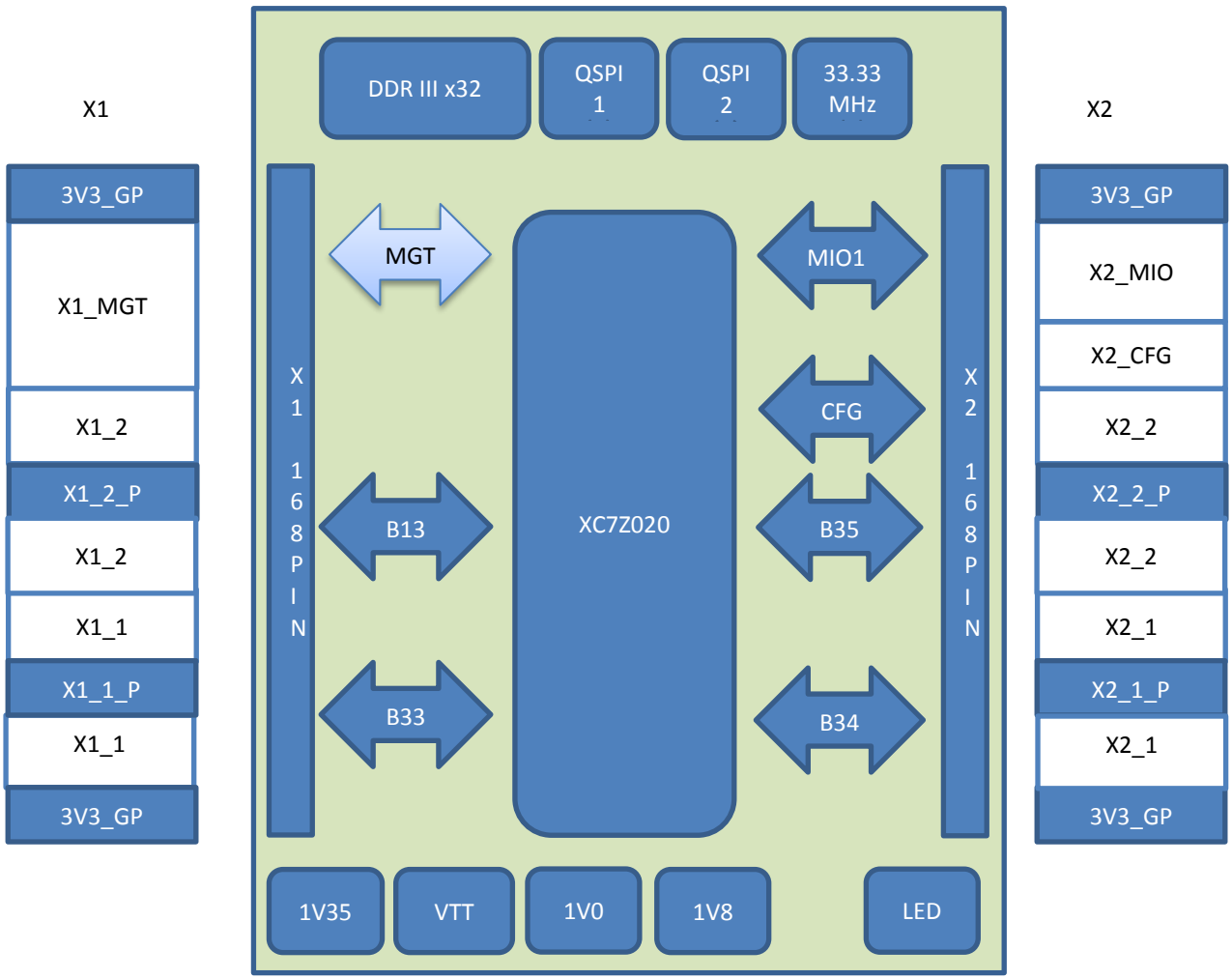
Further support to aid in customer specific design in's is available at competitive rates, please contact KR for details: + 41 61 545 2080 or mail to office@knowres.com

Introduction

With the KRM-3Z7020, KR provides a highly flexible and cost-efficient board for FPGA and embedded systems prototyping. Due to its low cost, the KRM-3Z7020 is also suitable for integration in low to mid volume end-products. It is based on a Xilinx Zynq 7Z020-XCLG484 SoC. The Xilinx SoC is accompanied by a 32 bit wide DDR3 memory subsystem, two instances of Quad SPI memory, power regulation, clock sources and 4 user LEDs.

The module's form-factor and pin assignment is fully compatible with the KRM-3Z7xxx specification which defines the module outline of 50mm x 70mm x 11mm (with heat spreader), 21W maximum Module power, and the standard pin out.

Block diagram



Board dimensions

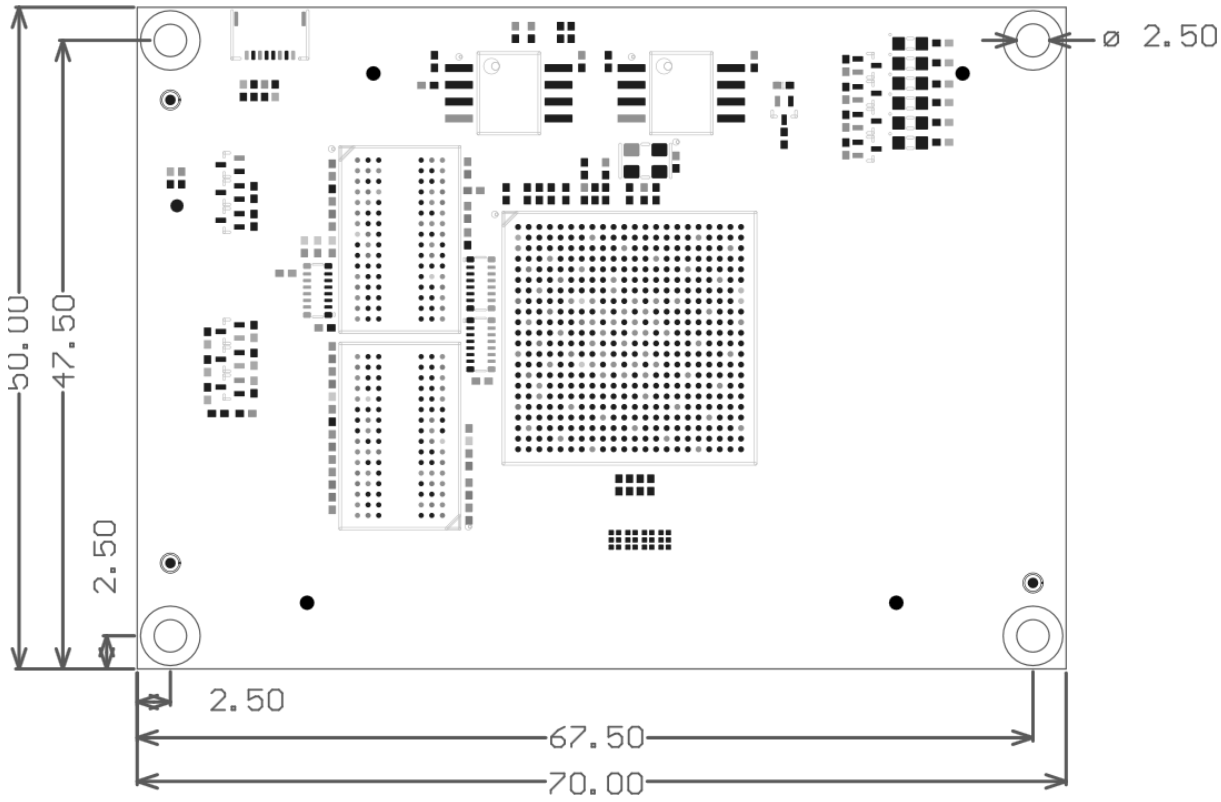


Figure 1: Board dimensions (in mm)

- Step Models of the module and its heat-spreader plate are available
- Altium PCB and Schematic templates are available

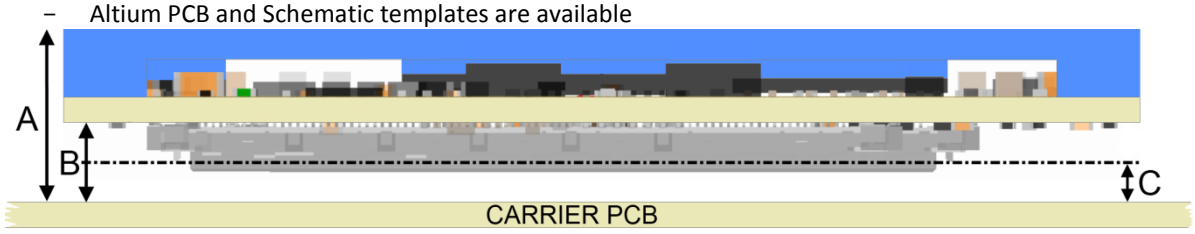


Figure 2: Board to board dimensions

- A = Height above carrier PCB ±0.2mm
- B = Mated stacking height
- C = Maximum component height area of carrier PCB.

Possible header variations:

– FX10A-168P-SV(85)	A = 10mm	B = 4mm	C = 1.5mm
– FX10A-168P-SV1(85)*	A = 11mm	B = 5mm	C = 2.5mm
– FX10A-168P-SV2(85)	A = 12mm	B = 6mm	C = 3.5mm
– FX10A-168P-SV3(85)	A = 13mm	B = 7mm	C = 4.5mm
– FX10A-168P-SV4(85)	A = 14mm	B = 8mm	C = 5.5mm

*KRC3701_CARRIER

Features

Overview

- Xilinx XC7Z020-1CLG484C
  - Available in speed grades 1 through 3; Commercial or industrial temperature range as options
  - 85k logic cells: 53’200 LUTs and 106’400 flip-flops
  - 220 DSP slices /18x25 MACCs
  - 140 x 36Kb block RAMs, a total of 560KB block RAM memory
  - Dual ARM A9 Cores with NEON co-processor
  - 256kB OC-RAM

- 4Gbit LDDR3 SDRAM

- 256Mbit QUAD SPI; 2 times 128Mbit

- 2x 168 pin Hirose FX10 dual row connectors
  - 4x PL I/O bank (Banks 13, 33, 34, 35)
    - 48 pins each
    - All byte groups (0-3) intact and length matched
    - I/O voltage supplied by carrier board, can be different for each bank
    - External I/O Voltage is switched; switch is enabled by on-board CFG_done
  - 1x PS MIO1 bank
    - MIO 16 through 53 (all of bank 501)
    - 1V8 default, supplied by KRM on-board regulator
  - JTAG chain to FPGA; 3V3
  - Configuration OK; buffered open collector output

- 33.333 MHz on-board oscillator

- 4 User LED driven by bank 34 & 35 I/O_0 and I/O_25 (not part of byte groups on I/O connector)

- Future use MGT pins for up to 8 lanes + 2 reference clocks
  -Not connected but reserved for Zynq 7Z030/45 module variants

Power supply and power considerations

Core power

-The KRM-3Z7020 requires a **stable** power supply of 3V3. In order to support designs with high FPGA utilization, a supply capable of providing at least 4A is required, 6A is recommended.
-Each of the 4 pin-groups of the 3V3 Global supply must be bypassed with a minimum of 47uF on the carrier board.
-Each Bank I/O supply must be bypassed with a minimum of 47uF on the carrier board.

I/O Bank Power sequence

I/O Bank power is to be supplied by the user design on the carrier board and may range from 1V35 to 3V3 for high-range banks or 1V35 to 1V8 for high-performance banks. Each I/O bank may be powered by a different I/O voltage, for maximum flexibility of the module.
In order to ensure optimal power sequencing of the power rails as recommended by Xilinx, the I/O Bank power is switched by on-board FET so that the user does not have to be concerned about the power sequencing of I/O voltages. The power-up of the I/O banks can be enabled by the "Pok" of the on board regulators or the "config-done" of the FPGA (an assembly option on the module)
The default power on of the I/O power rails is driven by the signal that indicates the completion of the FPGA configuration.

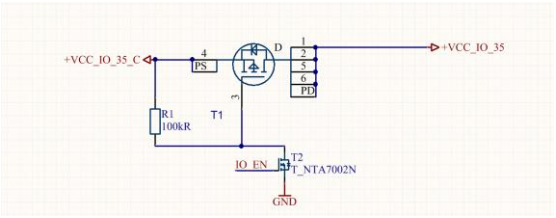


Figure 3

Supply Type	FX10 pin number	Voltage	Current	Remark
Global Module supply for internal regulators and CFG circuits	X1: 1,2, 165,166,167,168[i] X2: 1,2,3,4,165,166,167,168	3V3 Global	4.2A [ii]	Bypass each corner with at least 47uF on carrier
I/O Supply X1 GROUP1 (BANK 33)	X1:29,30	1V35 to 3V3	600mA [iii]	Bypass with at least 47uF on carrier
I/O Supply X1 GROUP2 (BANK 13)	X1:83,84	1V35 to 3V3	600mA	Bypass with at least 47uF on carrier
I/O Supply X2 GROUP1 (BANK 34)	X2: 31,32	1V35 to 1V8/3V3[iv]	600mA	Bypass with at least 47uF on carrier
I/O Supply X2 GROUP2 (BANK 35)	X2: 85,86	1V35 to 1V8/3V3[v]	600mA	Bypass with at least 47uF on carrier

[i] In order to ensure best performance with MGT capable modules, treat X1: 165-168 as low noise supply pins and isolate with a ferrite bead /capacitor Pi filter from other 3V3 rails.
[ii] The maximum core power to the Module is 14x 0.3A @3.3V = 13.86W.
[iii] The maximum I/O power to the module is 4x 0.6A @3.3V = 7.92W
[iv] Limit to 1V8 in order to ensure full compatibility with all modules of the KRM-3Z7xxx family
[v] Limit to 1V8 in order to ensure full compatibility with all modules of the KRM-3Z7xxx family

Clocking resources

Onboard oscillator

The onboard oscillator provides 33.33 MHz to the PS PLL of the SoC.

External PL Fabric clocks

Each bank exposes all clock capable pins, please consult the KRM-3Z7020 I/O tables and Xilinx clocking guide for details.

External MGT clocks (future use)

Two MGT clock inputs are provided through the FX10 connector interface. Details will be described in the datasheet of MGT capable modules.

Reset

-The PS reset port is available in the configuration and housekeeping signal group on connector X2: Pin115
-The reset pin is internally pulled up to 3V3 Global and forwarded to the PS reset pin via the BMC.
-Power-on-reset (PoR) is available via HW_RESET_IN on connector X2: Pin125.
-The module is kept in hardware reset until all voltages are stable.
-The module is self-resetting at power up, no external reset or power monitor is required or recommended.
-Unless there is an explicit need for a HW reset capability, tie pin X2:125 to GND.
-Reset_INn is best left unconnected or driven by an open drain source such as a JTAG adapter.

Signal name	FPGA pin	Board connector	Direction	Remark	I/O Level
RESET_INn	NA	X2: Pin115	FX10 → BMC ->FPGA	active low	INT PU to 3V3
HW_RESET_IN	NA	X2: Pin125	FX10 ->BMC -> FPGA	active high	3V3

Ready

-The module reports the conclusion of the configuration process via the signal CFG_OKn on connector X2:Pin116.
-CFG_OKn is a connected to a dedicated FET and implemented as an open drain output. It may sink as much as 50mA. An external pull-up resistor is required.
-CFG_OKn is provided by the BMC controller and derived from the Config-Done signal of the FPGA.
-CFG_OKn goes low after the FPGA/SoC has been configured successfully.

Signal name	FPGA pin	Board connector	Direction	Remark	I/O Level
CFG_OKn	NA	X2: Pin116	FPGA→ BMC -> FX10	active low	OC

VCCBATT_0

The VCCBATT_0 input is available via V_BATT_IN on connector X2: Pin126.

Signal name	FPGA pin	Board connector	Direction	Remark	I/O Level
V_BATT_IN	G9	X2: Pin126	X2 -> FPGA	active high	2V max

Configuration

JTAG Interface

The FPGA configuration file - i.e. the FPGA firmware - can be loaded via dedicated JTAG pins

	Signal name	Board connector	Direction	Remark	I/O Level
JTAG	TMS	X2:118	FX10 → FPGA		3V3
	TCK	X2:117	FX10 → FPGA		3V3
	TDO	X2:120	FPGA → FX10		3V3
	TDI	X2:119	FX10 → FPGA		3V3

Mode Pins

The MIO_0 Bank of the PS system (Bank 500) is not exposed on the modules I/O pins but dedicated to the modules internal functions such as configuration and housekeeping.
Mode pins MIO_02 through MIO_08 are largely dual-use; they determine the power-up-mode and are also used to implement the two QSPI interfaces.

The pin MIO_07 is used to set the MIO Bank0 to 3.3V. The pin MIO_08 is used to set the MIO Bank1 to 1.8V.A Board management Controller (BMC) is used to determine the Boot Source (SD-Card or QSPI), the Boot Mode (JTAG or Self) and to enable the PLL. By default, the Boot Source is set to SD-Card and the Boot Mode to Self. Thus, on power up, the system will boot automatically on the SD-Card.

It is possible to modify the Boot Source and the Boot Mode by sending the appropriate commands to the BMC through a serial connection. Please, refer to the document entitled *BMC_how_to_guide.pdf* for more information.

On-Board Quad SPI Configuration Memory

Two instances of QSPI memory are implemented on the module.

Each instance is populated with a 128Mbit QSPI flash.

	Signal name	MIO	Direction	Remark	I/O Level
QSPI0	S#	MIO_01	FPGA → SPI	Pull up on Module	3V3
	DQ0	MIO_02	BI-DIR		3V3
	DQ1	MIO_03	BI-DIR		3V3
	DQ2/W#	MIO_04	BI-DIR		3V3
	DQ3/HOLD#	MIO_05	BI-DIR		3V3
	CLK	MIO_06	FPGA → SPI		3V3

	Signal name	MIO	Direction	Remark	I/O Level
QSPI1	S#	MIO_00	FPGA → SPI	Pull up on Module	3V3
	DQ0	MIO_10	BI-DIR		3V3
	DQ1	MIO_11	BI-DIR		3V3
	DQ2/W#	MIO_12	BI-DIR		3V3
	DQ3/HOLD#	MIO_13	BI-DIR		3V3
	CLK	MIO_09	FPGA → SPI		3V3

DDR3 SDRAM

-The KRM-3Z7020 is populated with two DDR3 SDRAM providing a total of 4Gb of RAM, organized as 256 x 32 bit (1GB).
-The Memory subsystem can run as fast as 1066MT/s even on the slowest speed grade SoC.
-The KRM-3Z7020 implementation takes advantage of the lower power requirements of 1.35V operation.

I/O Headers

The KRM-3Z7020's I/O pinning is fully compatible with all future releases of KRM-3Z7xxx series modules.
Two Hirose FX10 168 pin connectors provide a total of 192 PL I/O signals, 38 PS MIO signals, 8MGT lanes, 2 differential MGT reference clocks, configuration and status pins.
Matching connectors for the carrier board design are:

- FX10A-168P-SVx

Please note HIROSE annotation is Pin **1a to 84a** and **1b to 84b**
This corresponds to KR annotation Pin **1 to 167** and **2 to 168**

	Group	FPGA Bank	Remark	I/O Level
X1	X1_1	Bank 33	3V3 supported on all modules	3V3
	X1_2	Bank 13	3V3 supported on all modules	3V3
	X1_MGT	NOT supported		3V3

	Group	FPGA Bank	Remark	I/O Level
X2	X2_1	Bank 34	3V3 supported but limit to 1V8 for full compatibility	1V8/3V3
	X2_2	Bank 35	3V3 supported but limit to 1V8 for full compatibility	1V8/3V3
	X2_CFG	CFG		3V3
	X2_MIO	MIO_1/501	1V8	1V8

PL BANKS

- The Byte-groups of a PL I/O bank (T0 –T3) are kept as a group and are length matched on the module.
- Differential I/O capable pins of the PL are routed as coupled differential pairs.

The I/O headers X1 and X2 feature I/O groups as defined by the KRM-3Z7xxx standard. The I/O groups are the same for each module of the KRM-3Z7xxx family but each module may map different ports to the I/O groups.
It is also permissible to not support MGT transceivers or to only support 4 of 8 MGT transceivers; all other I/O ports must be supported.
In order to be fully compatible with all available KRM-3Z7xxx modules, the X2 I/O banks should only use I/O voltages of 1V8 or less as some Modules will map **High performance** banks instead of **High range** banks onto X2.
If future module compatibility is not a concern, the full voltage range up to 3V3 may be utilized on all I/O banks of the KRM-3Z7020 module.

MIO BANK

The MIO I/O Bank voltage is 1V8. MIO signals 16 through 53 (Bank 501) are available. In order to be compatible with KR issued Linux BSP's we recommend using the MIO assignment as shown on one of the KR issued Evaluation boards such as the KRC3701 carrier. Naturally other configurations are possible, contact KR for BSP support of your desired configuration.

MGT BANK

NO MGT signals are available on the module. Treat the pins as RFU (reserved future use) or consult the datasheet of an MGT capable module in order to add MGT features on the carrier design.

Connector Schematic

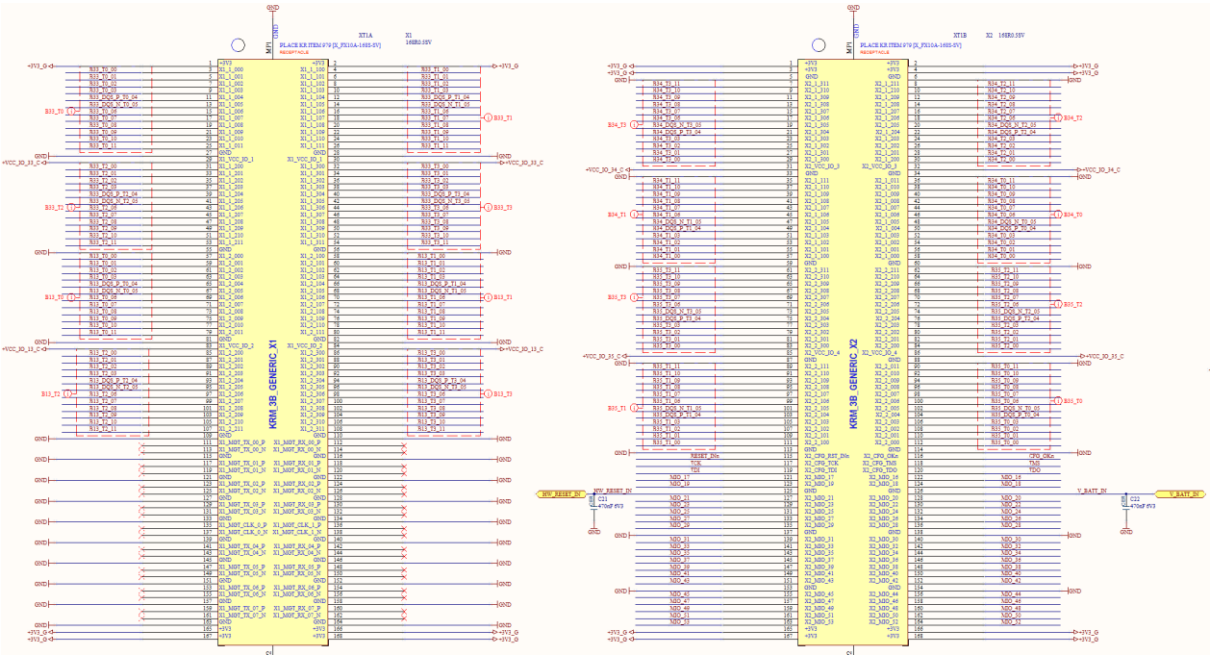


Figure 4

Pin Mapping

Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
X2:116	T12	DONE_0	NA	0	CONFIG	X1_CFG	OC	CFG_OKn after FET
X2:117	G11	TCK_0	NA	0	CONFIG	X1_CFG	3V3_Global	
X2:119	H13	TDI_0	NA	0	CONFIG	X1_CFG	3V3_Global	
X2:120	G14	TDO_0	NA	0	CONFIG	X1_CFG	3V3_Global	
X2:118	G12	TMS_0	NA	0	CONFIG	X1_CFG	3V3_Global	
NA	R7	IO_0_13	NA	13	HR	OB_SPARE	VIO_X1_2	NOT USED
X1:57	V10	IO_L1P_T0_13	0	13	HR	X1_2	VIO_X1_2	
X1:59	V9	IO_L1N_T0_13	0	13	HR	X1_2	VIO_X1_2	
X1:61	V8	IO_L2P_T0_13	0	13	HR	X1_2	VIO_X1_2	
X1:63	W8	IO_L2N_T0_13	0	13	HR	X1_2	VIO_X1_2	
X1:65	W11	IO_L3P_T0_DQS_13	0	13	HR	X1_2	VIO_X1_2	
X1:67	W10	IO_L3N_T0_DQS_13	0	13	HR	X1_2	VIO_X1_2	
X1:69	V12	IO_L4P_T0_13	0	13	HR	X1_2	VIO_X1_2	
X1:71	W12	IO_L4N_T0_13	0	13	HR	X1_2	VIO_X1_2	
X1:73	U12	IO_L5P_T0_13	0	13	HR	X1_2	VIO_X1_2	
X1:75	U11	IO_L5N_T0_13	0	13	HR	X1_2	VIO_X1_2	
X1:77	U10	IO_L6P_T0_13	0	13	HR	X1_2	VIO_X1_2	
X1:79	U9	IO_L6N_T0_VREF_13	0	13	HR	X1_2	VIO_X1_2	
X1:58	AA12	IO_L7P_T1_13	1	13	HR	X1_2	VIO_X1_2	
X1:60	AB12	IO_L7N_T1_13	1	13	HR	X1_2	VIO_X1_2	
X1:62	AA11	IO_L8P_T1_13	1	13	HR	X1_2	VIO_X1_2	
X1:64	AB11	IO_L8N_T1_13	1	13	HR	X1_2	VIO_X1_2	
X1:66	AB10	IO_L9P_T1_DQS_13	1	13	HR	X1_2	VIO_X1_2	
X1:68	AB9	IO_L9N_T1_DQS_13	1	13	HR	X1_2	VIO_X1_2	
X1:70	Y11	IO_L10P_T1_13	1	13	HR	X1_2	VIO_X1_2	
X1:72	Y10	IO_L10N_T1_13	1	13	HR	X1_2	VIO_X1_2	
X1:74	AA9	IO_L11P_T1_SRCC_13	1	13	HR	X1_2	VIO_X1_2	
X1:76	AA8	IO_L11N_T1_SRCC_13	1	13	HR	X1_2	VIO_X1_2	
X1:78	Y9	IO_L12P_T1_MRCC_13	1	13	HR	X1_2	VIO_X1_2	
X1:80	Y8	IO_L12N_T1_MRCC_13	1	13	HR	X1_2	VIO_X1_2	
X1:85	Y6	IO_L13P_T2_MRCC_13	2	13	HR	X1_2	VIO_X1_2	
X1:87	Y5	IO_L13N_T2_MRCC_13	2	13	HR	X1_2	VIO_X1_2	
X1:89	AA7	IO_L14P_T2_SRCC_13	2	13	HR	X1_2	VIO_X1_2	
X1:91	AA6	IO_L14N_T2_SRCC_13	2	13	HR	X1_2	VIO_X1_2	
X1:93	AB2	IO_L15P_T2_DQS_13	2	13	HR	X1_2	VIO_X1_2	
X1:95	AB1	IO_L15N_T2_DQS_13	2	13	HR	X1_2	VIO_X1_2	
X1:97	AB5	IO_L16P_T2_13	2	13	HR	X1_2	VIO_X1_2	
X1:99	AB4	IO_L16N_T2_13	2	13	HR	X1_2	VIO_X1_2	
X1:101	AB7	IO_L17P_T2_13	2	13	HR	X1_2	VIO_X1_2	

Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
X1:103	AB6	IO_L17N_T2_13	2	13	HR	X1_2	VIO_X1_2	
X1:105	Y4	IO_L18P_T2_13	2	13	HR	X1_2	VIO_X1_2	
X1:107	AA4	IO_L18N_T2_13	2	13	HR	X1_2	VIO_X1_2	
X1:86	R6	IO_L19P_T3_13	3	13	HR	X1_2	VIO_X1_2	
X1:88	T6	IO_L19N_T3_VREF_13	3	13	HR	X1_2	VIO_X1_2	
X1:90	T4	IO_L20P_T3_13	3	13	HR	X1_2	VIO_X1_2	
X1:92	U4	IO_L20N_T3_13	3	13	HR	X1_2	VIO_X1_2	
X1:94	V5	IO_L21P_T3_DQS_13	3	13	HR	X1_2	VIO_X1_2	
X1:96	V4	IO_L21N_T3_DQS_13	3	13	HR	X1_2	VIO_X1_2	
X1:98	U6	IO_L22P_T3_13	3	13	HR	X1_2	VIO_X1_2	
X1:100	U5	IO_L22N_T3_13	3	13	HR	X1_2	VIO_X1_2	
X1:102	V7	IO_L23P_T3_13	3	13	HR	X1_2	VIO_X1_2	
X1:104	W7	IO_L23N_T3_13	3	13	HR	X1_2	VIO_X1_2	
X1:106	W6	IO_L24P_T3_13	3	13	HR	X1_2	VIO_X1_2	
X1:108	W5	IO_L24N_T3_13	3	13	HR	X1_2	VIO_X1_2	
NA	U7	IO_25_13	NA	13	HR	OB_SPARE	VIO_X1_2	NOT USED
NA	U19	IO_0_33	NA	33	HR	OB_SPARE	VIO_X1_1	NOT USED
X1:3	T21	IO_L1P_T0_33	0	33	HR	X1_1	VIO_X1_1	
X1:5	U21	IO_L1N_T0_33	0	33	HR	X1_1	VIO_X1_1	
X1:7	T22	IO_L2P_T0_33	0	33	HR	X1_1	VIO_X1_1	
X1:9	U22	IO_L2N_T0_33	0	33	HR	X1_1	VIO_X1_1	
X1:11	V22	IO_L3P_T0_DQS_33	0	33	HR	X1_1	VIO_X1_1	
X1:13	W22	IO_L3N_T0_DQS_33	0	33	HR	X1_1	VIO_X1_1	
X1:15	W20	IO_L4P_T0_33	0	33	HR	X1_1	VIO_X1_1	
X1:17	W21	IO_L4N_T0_33	0	33	HR	X1_1	VIO_X1_1	
X1:19	U20	IO_L5P_T0_33	0	33	HR	X1_1	VIO_X1_1	
X1:21	V20	IO_L5N_T0_33	0	33	HR	X1_1	VIO_X1_1	
X1:23	V18	IO_L6P_T0_33	0	33	HR	X1_1	VIO_X1_1	
X1:25	V19	IO_L6N_T0_VREF_33	0	33	HR	X1_1	VIO_X1_1	
X1:4	AA22	IO_L7P_T1_33	1	33	HR	X1_1	VIO_X1_1	
X1:6	AB22	IO_L7N_T1_33	1	33	HR	X1_1	VIO_X1_1	
X1:8	AA21	IO_L8P_T1_33	1	33	HR	X1_1	VIO_X1_1	
X1:10	AB21	IO_L8N_T1_33	1	33	HR	X1_1	VIO_X1_1	
X1:12	Y20	IO_L9P_T1_DQS_33	1	33	HR	X1_1	VIO_X1_1	
X1:14	Y21	IO_L9N_T1_DQS_33	1	33	HR	X1_1	VIO_X1_1	
X1:16	AB19	IO_L10P_T1_33	1	33	HR	X1_1	VIO_X1_1	
X1:18	AB20	IO_L10N_T1_33	1	33	HR	X1_1	VIO_X1_1	
X1:20	Y19	IO_L11P_T1_SRCC_33	1	33	HR	X1_1	VIO_X1_1	
X1:22	AA19	IO_L11N_T1_SRCC_33	1	33	HR	X1_1	VIO_X1_1	
X1:24	Y18	IO_L12P_T1_MRCC_33	1	33	HR	X1_1	VIO_X1_1	
X1:26	AA18	IO_L12N_T1_MRCC_33	1	33	HR	X1_1	VIO_X1_1	

Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
X1:31	W17	IO_L13P_T2_MRCC_33	2	33	HR	X1_1	VIO_X1_1	
X1:33	W18	IO_L13N_T2_MRCC_33	2	33	HR	X1_1	VIO_X1_1	
X1:35	W16	IO_L14P_T2_SRCC_33	2	33	HR	X1_1	VIO_X1_1	
X1:37	Y16	IO_L14N_T2_SRCC_33	2	33	HR	X1_1	VIO_X1_1	
X1:39	U15	IO_L15P_T2_DQS_33	2	33	HR	X1_1	VIO_X1_1	
X1:41	U16	IO_L15N_T2_DQS_33	2	33	HR			
X1:43	U17	IO_L16P_T2_33	2	33	HR	X1_1	VIO_X1_1	
X1:45	V17	IO_L16N_T2_33	2	33	HR	X1_1	VIO_X1_1	
X1:47	AA17	IO_L17P_T2_33	2	33	HR	X1_1	VIO_X1_1	
X1:49	AB17	IO_L17N_T2_33	2	33	HR	X1_1	VIO_X1_1	
X1:51	AA16	IO_L18P_T2_33	2	33	HR	X1_1	VIO_X1_1	
X1:53	AB16	IO_L18N_T2_33	2	33	HR	X1_1	VIO_X1_1	
X1:32	V14	IO_L19P_T3_33	3	33	HR	X1_1	VIO_X1_1	
X1:34	V15	IO_L19N_T3_VREF_33	3	33	HR	X1_1	VIO_X1_1	
X1:36	V13	IO_L20P_T3_33	3	33	HR	X1_1	VIO_X1_1	
X1:38	W13	IO_L20N_T3_33	3	33	HR	X1_1	VIO_X1_1	
X1:40	W15	IO_L21P_T3_DQS_33	3	33	HR	X1_1	VIO_X1_1	
X1:42	Y15	IO_L21N_T3_DQS_33	3	33	HR	X1_1	VIO_X1_1	
X1:44	Y14	IO_L22P_T3_33	3	33	HR	X1_1	VIO_X1_1	
X1:46	AA14	IO_L22N_T3_33	3	33	HR	X1_1	VIO_X1_1	
X1:48	Y13	IO_L23P_T3_33	3	33	HR	X1_1	VIO_X1_1	
X1:50	AA13	IO_L23N_T3_33	3	33	HR	X1_1	VIO_X1_1	
X1:52	AB14	IO_L24P_T3_33	3	33	HR	X1_1	VIO_X1_1	
X1:54	AB15	IO_L24N_T3_33	3	33	HR	X1_1	VIO_X1_1	
NA	U14	IO_25_33	NA	33	HR	OB_SPARE	VIO_X1_1	NOT USED
NA	H15	IO_0_34	NA	34	HR	OB_LED	VIO_X2_1	USR_LED_2
X2:58	J15	IO_L1P_T0_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:56	K15	IO_L1N_T0_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:54	J16	IO_L2P_T0_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:52	J17	IO_L2N_T0_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:50	K16	IO_L3P_T0_DQS_PUDC_B_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:48	L16	IO_L3N_T0_DQS_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:46	L17	IO_L4P_T0_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:44	M17	IO_L4N_T0_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:42	N17	IO_L5P_T0_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:40	N18	IO_L5N_T0_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:38	M15	IO_L6P_T0_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:36	M16	IO_L6N_T0_VREF_34	0	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:57	J18	IO_L7P_T1_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:55	K18	IO_L7N_T1_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:53	J21	IO_L8P_T1_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC

Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
X2:51	J22	IO_L8N_T1_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:49	J20	IO_L9P_T1_DQS_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:47	K21	IO_L9N_T1_DQS_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:45	L21	IO_L10P_T1_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:43	L22	IO_L10N_T1_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:41	K19	IO_L11P_T1_SRCC_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:39	K20	IO_L11N_T1_SRCC_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:37	L18	IO_L12P_T1_MRCC_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:35	L19	IO_L12N_T1_MRCC_34	1	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:30	M19	IO_L13P_T2_MRCC_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:28	M20	IO_L13N_T2_MRCC_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:26	N19	IO_L14P_T2_SRCC_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:24	N20	IO_L14N_T2_SRCC_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:22	M21	IO_L15P_T2_DQS_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:20	M22	IO_L15N_T2_DQS_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:18	N22	IO_L16P_T2_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:16	P22	IO_L16N_T2_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:14	R20	IO_L17P_T2_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:12	R21	IO_L17N_T2_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:10	P20	IO_L18P_T2_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:8	P21	IO_L18N_T2_34	2	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:29	N15	IO_L19P_T3_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:27	P15	IO_L19N_T3_VREF_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:25	P17	IO_L20P_T3_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:23	P18	IO_L20N_T3_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:21	T16	IO_L21P_T3_DQS_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:19	T17	IO_L21N_T3_DQS_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:17	R19	IO_L22P_T3_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:15	T19	IO_L22N_T3_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:13	R18	IO_L23P_T3_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:11	T18	IO_L23N_T3_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:9	P16	IO_L24P_T3_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
X2:7	R16	IO_L24N_T3_34	3	34	HR	X2_1	VIO_X2_1	1V8_FC
NA	R15	IO_25_34	NA	34	HR	OB_LED	VIO_X2_1	USR_LED_1
NA	H17	IO_0_35	NA	35	HR	OB_LED	VIO_X2_2	USR_LED_4
X2:112	F16	IO_L1P_T0_AD0P_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:110	E16	IO_L1N_T0_AD0N_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:108	D16	IO_L2P_T0_AD8P_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:106	D17	IO_L2N_T0_AD8N_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:104	E15	IO_L3P_T0_DQS_AD1P_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:102	D15	IO_L3N_T0_DQS_AD1N_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC

Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
X2:100	G15	IO_L4P_T0_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:98	G16	IO_L4N_T0_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:96	F18	IO_L5P_T0_AD9P_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:94	E18	IO_L5N_T0_AD9N_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:92	G17	IO_L6P_T0_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:90	F17	IO_L6N_T0_VREF_35	0	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:111	C15	IO_L7P_T1_AD2P_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:109	B15	IO_L7N_T1_AD2N_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:107	B16	IO_L8P_T1_AD10P_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:105	B17	IO_L8N_T1_AD10N_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:103	A16	IO_L9P_T1_DQS_AD3P_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:101	A17	IO_L9N_T1_DQS_AD3N_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:99	A18	IO_L10P_T1_AD11P_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:97	A19	IO_L10N_T1_AD11N_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:95	C17	IO_L11P_T1_SRCC_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:93	C18	IO_L11N_T1_SRCC_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:91	D18	IO_L12P_T1_MRCC_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:89	C19	IO_L12N_T1_MRCC_35	1	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:84	B19	IO_L13P_T2_MRCC_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:82	B20	IO_L13N_T2_MRCC_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:80	D20	IO_L14P_T2_AD4P_SRCC_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:78	C20	IO_L14N_T2_AD4N_SRCC_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:76	A21	IO_L15P_T2_DQS_AD12P_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:74	A22	IO_L15N_T2_DQS_AD12N_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:72	D22	IO_L16P_T2_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:70	C22	IO_L16N_T2_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:68	E21	IO_L17P_T2_AD5P_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:66	D21	IO_L17N_T2_AD5N_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:64	B21	IO_L18P_T2_AD13P_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:62	B22	IO_L18N_T2_AD13N_35	2	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:83	H19	IO_L19P_T3_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:81	H20	IO_L19N_T3_VREF_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:79	G19	IO_L20P_T3_AD6P_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:77	F19	IO_L20N_T3_AD6N_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:75	E19	IO_L21P_T3_DQS_AD14P_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:73	E20	IO_L21N_T3_DQS_AD14N_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:71	G20	IO_L22P_T3_AD7P_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:69	G21	IO_L22N_T3_AD7N_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:67	F21	IO_L23P_T3_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC

Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
X2:65	F22	IO_L23N_T3_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:63	H22	IO_L24P_T3_AD15P_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC
X2:61	G22	IO_L24N_T3_AD15N_35	3	35	HR	X2_2	VIO_X2_2	1V8_FC
NA	H18	IO_25_35	NA	35	HR	OB_LED	VIO_X2_2	USR_LED_3
NA	F7	PS_CLK_500	NA	500	MIO	OB_INT	3V3_Global	
NA	F8	PS_MIO_VREF_501	NA	501	MIO	OB_P	1V8_OB	
NA	B5	PS_POR_B_500	NA	500	MIO	OB_INT	3V3_Global	Internal P_OK
NA	E6	PS_MIO15_500	NA	500	MIO	OB_MIO	3V3_Global	
X2:121	E9	PS_MIO17_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:123	E10	PS_MIO19_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:127	F11	PS_MIO21_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:129	E11	PS_MIO23_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:131	F12	PS_MIO25_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:133	D7	PS_MIO27_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:135	E8	PS_MIO29_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:139	F9	PS_MIO31_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:141	G13	PS_MIO33_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:143	F14	PS_MIO35_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:148	F13	PS_MIO38_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:150	E14	PS_MIO40_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:152	D8	PS_MIO42_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:156	E13	PS_MIO44_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:158	D12	PS_MIO46_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:160	D11	PS_MIO48_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:162	D13	PS_MIO50_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:164	D10	PS_MIO52_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:115	C9	PS_SRST_B_501	NA	501	MIO	X2_MIO	Int PU	Ext OC/OD
NA	B6	PS_MIO14_500	NA	500	MIO	X2_MIO	3V3_Global	
X2:122	D6	PS_MIO16_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:124	A7	PS_MIO18_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:128	A8	PS_MIO20_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:130	A14	PS_MIO22_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:132	B7	PS_MIO24_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:134	A13	PS_MIO26_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:136	A12	PS_MIO28_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:140	A11	PS_MIO30_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:142	C7	PS_MIO32_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:144	B12	PS_MIO34_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:146	A9	PS_MIO36_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:145	B14	PS_MIO37_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC
X2:147	C13	PS_MIO39_501	NA	501	MIO	X2_MIO	1V8_OB	1V8_FC

Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
X2:149	C8	PS_MIO41_501	NA	501	MIO	X2_MIO	1V8_OB	
X2:151	B11	PS_MIO43_501	NA	501	MIO	X2_MIO	1V8_OB	
X2:155	B9	PS_MIO45_501	NA	501	MIO	X2_MIO	1V8_OB	
X2:157	B10	PS_MIO47_501	NA	501	MIO	X2_MIO	1V8_OB	
X2:159	C14	PS_MIO49_501	NA	501	MIO	X2_MIO	1V8_OB	
X2:161	C10	PS_MIO51_501	NA	501	MIO	X2_MIO	1V8_OB	
X2:163	C12	PS_MIO53_501	NA	501	MIO	X2_MIO	1V8_OB	
NA	A6	PS_MIO13_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	C5	PS_MIO12_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	B4	PS_MIO11_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	G7	PS_MIO10_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	C4	PS_MIO9_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	E5	PS_MIO8_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	D5	PS_MIO7_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	A4	PS_MIO6_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	A3	PS_MIO5_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	E4	PS_MIO4_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	F6	PS_MIO3_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	A2	PS_MIO2_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	A1	PS_MIO1_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	G6	PS_MIO0_500	NA	500	MIO	OB_MIO	3V3_Global	
NA	R12	VCCO_0	NA	0	NA	NA	3V3_Global	
NA	AA10	VCCO_13	NA	13	NA		VIO_X1_2	
NA	AB3	VCCO_13	NA	13	NA		VIO_X1_2	
NA	T5	VCCO_13	NA	13	NA		VIO_X1_2	
NA	U8	VCCO_13	NA	13	NA		VIO_X1_2	
NA	V11	VCCO_13	NA	13	NA		VIO_X1_2	
NA	W4	VCCO_13	NA	13	NA		VIO_X1_2	
NA	Y7	VCCO_13	NA	13	NA		VIO_X1_2	
NA	AA20	VCCO_33	NA	33	NA		VIO_X1_1	
NA	AB13	VCCO_33	NA	33	NA		VIO_X1_1	
NA	U18	VCCO_33	NA	33	NA		VIO_X1_1	
NA	V21	VCCO_33	NA	33	NA		VIO_X1_1	
NA	W14	VCCO_33	NA	33	NA		VIO_X1_1	
NA	Y17	VCCO_33	NA	33	NA		VIO_X1_1	
NA	K17	VCCO_34	NA	34	NA		VIO_X2_1	1V8_FC
NA	L20	VCCO_34	NA	34	NA		VIO_X2_1	1V8_FC
NA	N16	VCCO_34	NA	34	NA		VIO_X2_1	1V8_FC
NA	P19	VCCO_34	NA	34	NA		VIO_X2_1	1V8_FC
NA	R22	VCCO_34	NA	34	NA		VIO_X2_1	1V8_FC
NA	T15	VCCO_34	NA	34	NA		VIO_X2_1	1V8_FC

Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
NA	A20	VCCO_35	NA	35	NA		VIO_X2_2	1V8_FC
NA	C16	VCCO_35	NA	35	NA		VIO_X2_2	1V8_FC
NA	D19	VCCO_35	NA	35	NA		VIO_X2_2	1V8_FC
NA	E22	VCCO_35	NA	35	NA		VIO_X2_2	1V8_FC
NA	F15	VCCO_35	NA	35	NA		VIO_X2_2	1V8_FC
NA	G18	VCCO_35	NA	35	NA		VIO_X2_2	1V8_FC
NA	H21	VCCO_35	NA	35	NA		VIO_X2_2	1V8_FC
NA	B3	VCCO_MIO0_500	NA	500	NA		3V3_Global	
NA	C6	VCCO_MIO0_500	NA	500	NA		3V3_Global	
X1:27	NA	GND	NA	NA	NA		GND	
X1:28	NA	GND	NA	NA	NA		GND	
X1:55	NA	GND	NA	NA	NA		GND	
X1:56	NA	GND	NA	NA	NA		GND	
X1:81	NA	GND	NA	NA	NA		GND	
X1:82	NA	GND	NA	NA	NA		GND	
X1:109	NA	GND	NA	NA	NA		GND	MGT FU
X1:110	NA	GND	NA	NA	NA		GND	MGT FU
X1:115	NA	GND	NA	NA	NA		GND	MGT FU
X1:116	NA	GND	NA	NA	NA		GND	MGT FU
X1:121	NA	GND	NA	NA	NA		GND	MGT FU
X1:122	NA	GND	NA	NA	NA		GND	MGT FU
X1:127	NA	GND	NA	NA	NA		GND	MGT FU
X1:128	NA	GND	NA	NA	NA		GND	MGT FU
X1:133	NA	GND	NA	NA	NA		GND	MGT FU
X1:134	NA	GND	NA	NA	NA		GND	MGT FU
X1:139	NA	GND	NA	NA	NA		GND	MGT FU
X1:140	NA	GND	NA	NA	NA		GND	MGT FU
X1:145	NA	GND	NA	NA	NA		GND	MGT FU
X1:146	NA	GND	NA	NA	NA		GND	MGT FU
X1:151	NA	GND	NA	NA	NA		GND	MGT FU
X1:152	NA	GND	NA	NA	NA		GND	MGT FU
X1:157	NA	GND	NA	NA	NA		GND	MGT FU
X1:158	NA	GND	NA	NA	NA		GND	MGT FU
X1:163	NA	GND	NA	NA	NA		GND	MGT FU
X1:164	NA	GND	NA	NA	NA		GND	MGT FU
X2:5	NA	GND	NA	NA	NA		GND	
X2:6	NA	GND	NA	NA	NA		GND	
X2:33	NA	GND	NA	NA	NA		GND	
X2:34	NA	GND	NA	NA	NA		GND	
X2:59	NA	GND	NA	NA	NA		GND	
X2:60	NA	GND	NA	NA	NA		GND	

Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
X2:87	NA	GND	NA	NA	NA		GND	
X2:88	NA	GND	NA	NA	NA		GND	
X2:113	NA	GND	NA	NA	NA		GND	
X2:114	NA	GND	NA	NA	NA		GND	
X2:125	NA	HW_RESET_IN	NA	NA	NA		NA	
X2:126	G9	V_BATT_IN	NA	NA	NA		NA	2.0V max
X2:137	NA	GND	NA	NA	NA		GND	
X2:138	NA	GND	NA	NA	NA		GND	
X2:153	NA	GND	NA	NA	NA		GND	
X2:154	NA	GND	NA	NA	NA		GND	
X2:1	NA	3V3_in	NA	NA	NA		3V3_in	
X2:2	NA	3V3_in	NA	NA	NA		3V3_in	
X2:3	NA	3V3_in	NA	NA	NA		3V3_in	
X2:4	NA	3V3_in	NA	NA	NA		3V3_in	
X2:165	NA	3V3_in	NA	NA	NA		3V3_in	
X2:166	NA	3V3_in	NA	NA	NA		3V3_in	
X2:167	NA	3V3_in	NA	NA	NA		3V3_in	
X2:168	NA	3V3_in	NA	NA	NA		3V3_in	
X1:1	NA	3V3_in	NA	NA	NA		3V3_in	
X1:2	NA	3V3_in	NA	NA	NA		3V3_in	
X1:165	NA	3V3_in	NA	NA	NA		3V3_in	MGT FU
X1:166	NA	3V3_in	NA	NA	NA		3V3_in	MGT FU
X1:167	NA	3V3_in	NA	NA	NA		3V3_in	MGT FU
X1:168	NA	3V3_in	NA	NA	NA		3V3_in	MGT FU
X1:83	NA	VCC_O_13	NA	13	X1_2_P		VIO_X1_2	SWITCHED
X1:84	NA	VCC_O_13	NA	13	X1_2_P		VIO_X1_2	SWITCHED
X1:29	NA	VCC_O_33	NA	33	X1_1_P		VIO_X1_1	SWITCHED
X1:30	NA	VCC_O_33	NA	33	X1_1_P		VIO_X1_1	SWITCHED
X2:31	NA	VCC_O_34	NA	34	X2_1_P		VIO_X2_1	SWITCHED 1V8_FC
X2:32	NA	VCC_O_34	NA	34	X2_1_P		VIO_X2_1	SWITCHED 1V8_FC
X2:85	NA	VCC_O_35	NA	35	X2_2_P		VIO_X2_2	SWITCHED 1V8_FC
X2:86	NA	VCC_O_35	NA	35	X2_2_P		VIO_X2_2	SWITCHED 1V8_FC

Compliance

All KRM modules are ROHSII and REACH compliant. For further details, customers may request the current declaration of conformity by emailing office@knowres.ch.
All KRM Modules are manufactured with UL94V-0 flammability rated PCBs with an IPC Class2 quality rating.

Electrical Specification

ESD

KRM Modules are sensitive to electrostatic discharge and must be handled with proper ESD precautions.

Absolute Maximum Ratings[vi]

Symbol	Description	Min	Max
POWER_IN	Global power in	-0V5	3V6
VCCO_12/13	HR Bank I/O power supply	-0V5	3V6
VCCO_34/35	HP Bank I/O power supply	-0V5	2V0
V_BATT_IN	Encryption key storage supply	-0V5	2V0
PS_IO	MIO Bank I/O signal levels	-0V5	2V0
PL_IO_HP	HP Bank I/O signal levels	-0V5	2V0
PL_IO_HR	HR Bank I/O signal levels	-0V5	3V6

Recommended Operating conditions

Symbol	Description	Min	Typ	Max
POWER_IN	Global power in	3V2	3V3	3V4
VCCO_12/13	HR Bank I/O power supply	3V2	3V3	3V4
VCCO_34/35	HP Bank I/O power supply	1V7	1V8	1V89
V_BATT_IN	Encryption key storage supply	1V0	--	1V89
PS_IO	MIO Bank I/O signal levels[vii]	-0V2	--	VCCO + 0V2
PL_IO_HP	HP Bank I/O signal levels	-0V2	--	VCCO + 0V2
PL_IO_HR	HR Bank I/O signal levels	-0V2	--	VCCO + 0V2

[vi] Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied.
Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect module reliability
[vii] For I/O operation, refer to the Xilinx *7 Series FPGAs SelectIO Resources User Guide* (UG471) or the Xilinx *Zynq-7000 SoC Technical Reference Manual* (UG585).

Thermal specification

Absolute Maximum Ratings[viii]

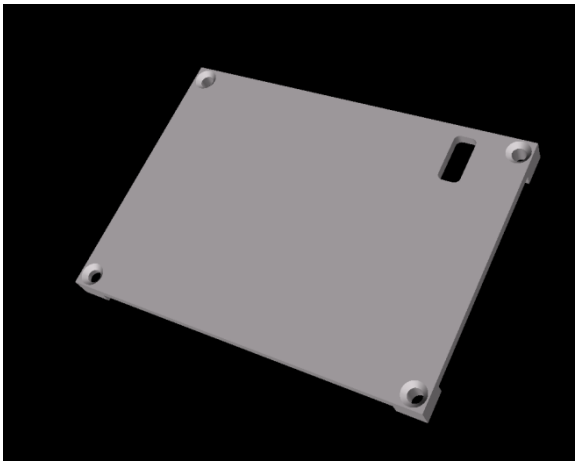
Symbol	Description	Min	Max
Delta T	Max temperature change per second while operating	--	+/-1°C/sec
TSTG	Storage temperature ambient un-powered	-40°C	+125°C

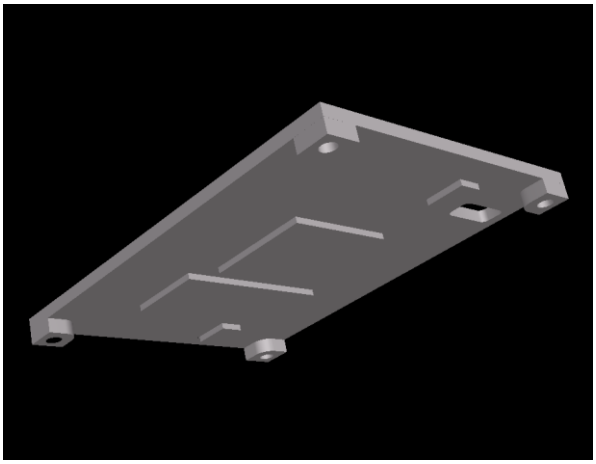
Recommended Operating Conditions

Symbol	Description	Min	Typ	Max
Tj C	Operating Junction temperature of FPGA for commercial grade	0°C	--	+70°C
Tj I	Operating Junction temperature of FPGA for industrial grade	-40°C	--	+85°C
Delta T	Allowed temperature change per second while operating	--	--	+/-0.5°C/sec

Heat Management

The thermal load of the Module depends greatly on the user application, and is driven by clock speed, toggle rate, logic utilization, active peripherals and CPU utilization. The user must ensure that the generated heat is adequately removed from the module so that the Recommended Operating Conditions are not exceeded.
In order to ensure a consistent thermal interface across all KRM-3xxx module variants, KR offers a module-specific heat-spreader plate. The plate is simply an adapter and is not designed as a standalone cooling solution. In some low power applications of the smaller module variants, the spreader plate may be sufficient as a standalone solution.





[viii] Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied.

Module configurations

The KRM3-Z7xxx Modules can be purchased in a multitude of configurations as shown in the table below. Option codes shown in black are valid options for this family, not all valid options may be combined (for example boot option set to on-board QSPI, but no Flash populated is invalid). Blue option codes may become future options of this module family or may apply to a different version.

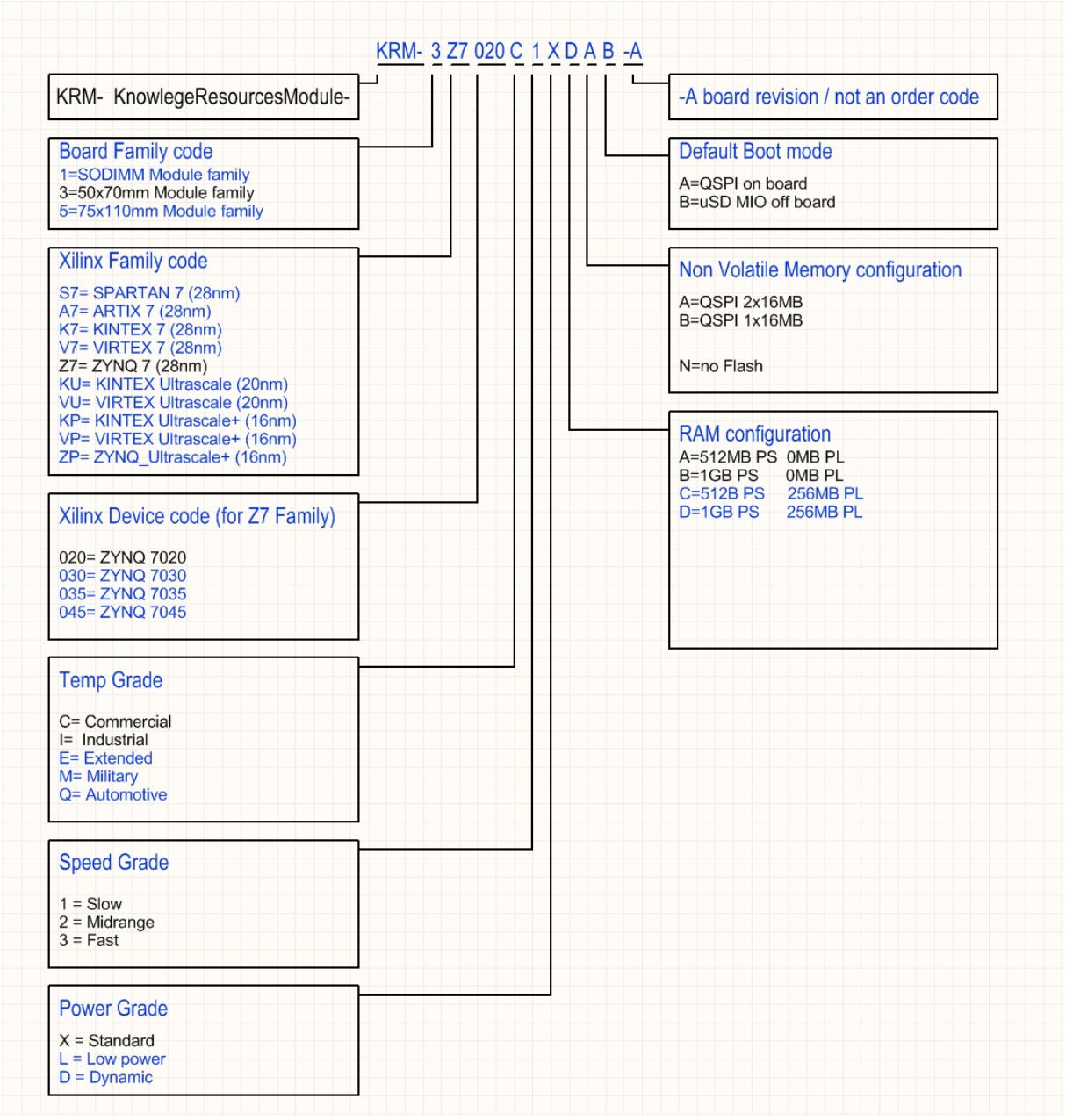
Standard Low quantity configuration

The standard assembly variant, which is orderable as samples, is as follows:

KRM-3Z7020C1XBAB-F

50x70mm module family, with a Zynq 7020, commercial speed grade, standard power rating, 1GB PS RAM and dual QSPI (32MB total) populated and boot mode set to external SD card interface.

Configuration table



Module Identification

Xilinx is no longer labeling its parts with speed grade and temperature grade information. The KRM PCB is also only labelled with the generic family code and contains no clear text information about its configuration. This makes it all but impossible to identify the modules detailed configuration.

All modules as of Board Rev_E can be identified by scanning the QR code label that is mounted on the PS DDR memory components. The QR code contains a unique URL that will query the database of the KR test system and will produce a PDF document that contains information about the factory configuration of the module and test sequence the module passed after production.

Errata

No known errata at the time of writing