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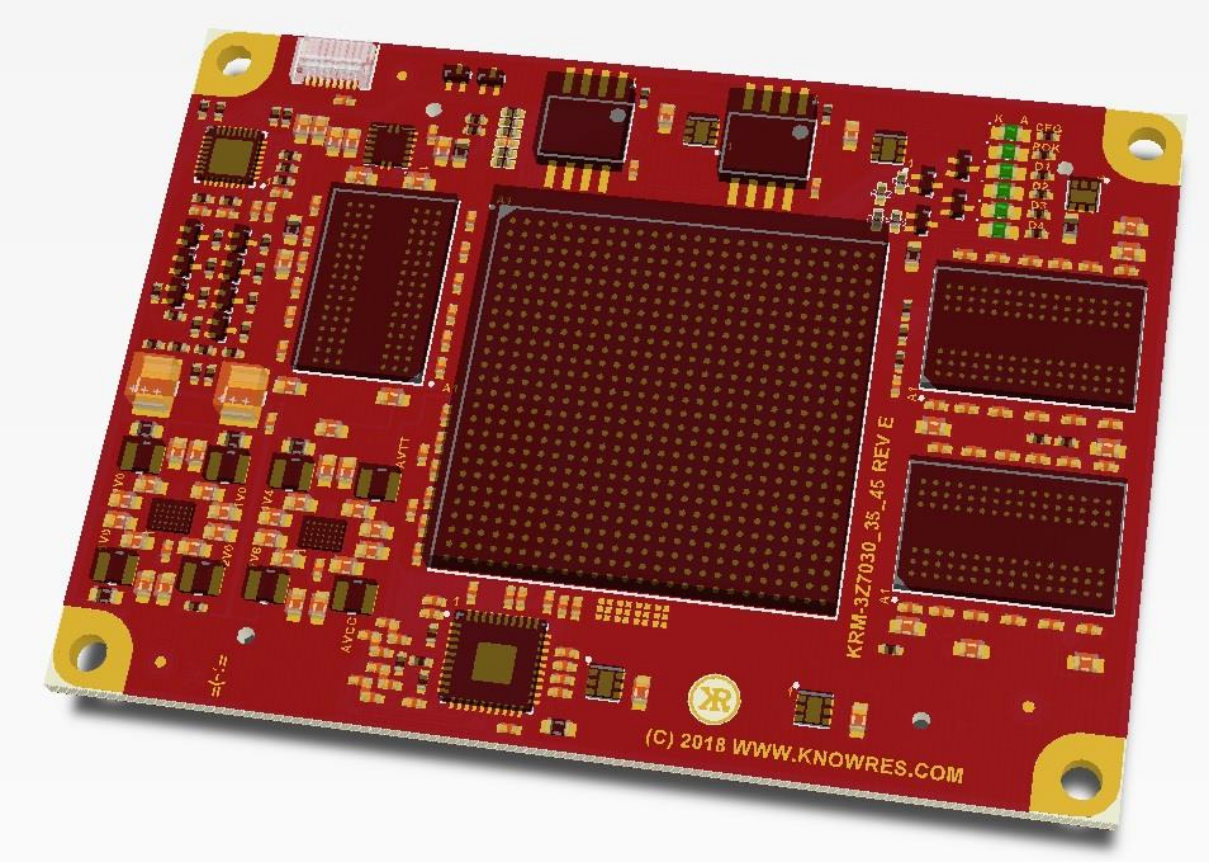
KRM-3Z7030-045

Data sheet Rev 1.9



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Revision History

Date	Document revision	HW revision	Changes
March 10th 2014	1.0	REV A	Initial document
March 17th 2014	1.1	REV A	Updated chapters on I/O bank power & I/O signal groups
March 20th 2014	1.2	REV A	Disclaimer and board to board dimension added
December 3rd 2014	1.3	REV A	Minor Corrections
December 16th 2014	1.4	REV A	Minor Corrections
August 27th 2015	1.5	REV A	Updated connector schematic, added Hirose annotation reference
February 12th 2016	1.6	REV A	Changed nomenclature to KRM-3Z7XXX Unified Datasheet of 30/35and 45 assembly variant Updated mounting hole diameter to 2mm Added Module configuration chapter Added Errata
November 7th 2019	1.7	REV E/F	Added Board Management Controller information Updated Acronyms part Updated Mode pins part Updated Reset part with HW_RESET_IN Added VCCBATT_0 part Updated Connector Schematic with HW_RESET_IN and V_BATT_IN pins Updated Pin Mapping part with HW_RESET_IN and V_BATT_IN Updated illustration in title part to Rev_E Updated Board Dimensions Added Compliance section Added Maximum ratings and recommended operating conditions Added FBG options in configuration table
November 29th 2019	1.8	REV_E/F	Removed obsolete web links Generalized Xilinx SoC Type with reference to Module configurations Updated reset recommendations Added reference to PL DDR3 of older board revisions Added reference to QR code for module identification Typographical edits
February 13rd 2020	1.9	REV_E/F	Corrected hyperlinks

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Assumptions

The reader is familiar with Xilinx FPGA and SoC components and the related terminology in common use.

Acronyms

FOM:	FPGA on Module
FU:	Future Use
KR:	Knowledge Resources GmbH
MIG:	Memory Interface Generator, a tool of Xilinx to easily implement a DDR3 controller
NA:	Not Applicable
PL:	Programmable Logic
PS:	Processing Subsystem
SoC:	System on Chip
BMC:	Board Management Controller

Reference documents

ZYNQ all programmable SoC, Xilinx, www.xilinx.com

Support

KR will provide free of charge to qualified customers:

-Schematic and PCB libraries with Module and carrier board design components (Altium)
-3D STEP models of the module and heat spreader plate
-LINUX BSP and LINUX port (Plug and Boot ready)
-Reference schematics of the evaluation boards (Altium native and PDF)
-Reference designs for on-board PL memory use
-Project scripts for Vivado to accelerate design starts

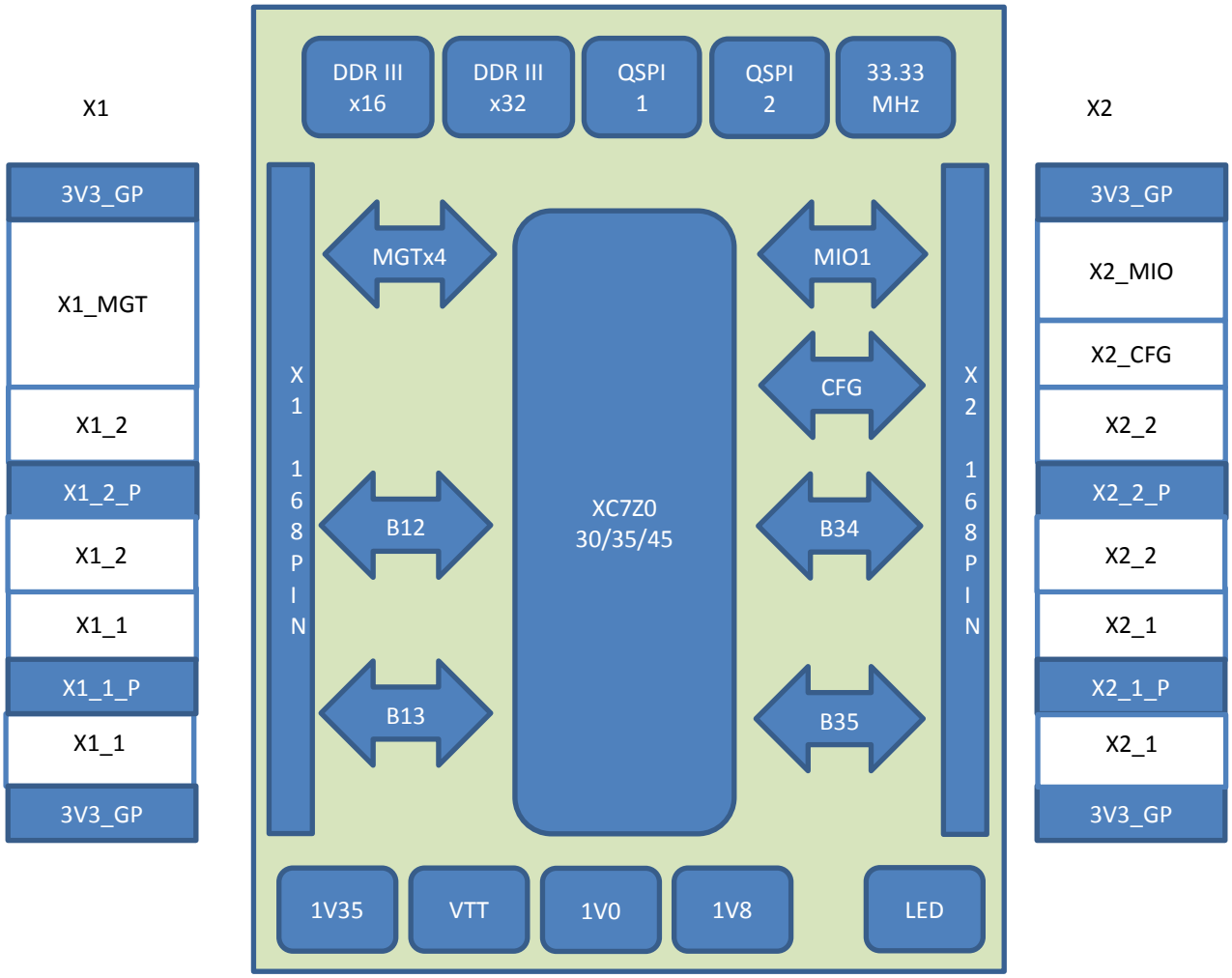
Further support to aid in customer specific design in's is available at competitive rates, please contact KR for details: + 41 61 545 2080 or mail to office@knowres.com

Introduction

With the KRM-3Z7xxx, KR provides a highly flexible and cost-efficient board for FPGA and embedded systems prototyping. Due to its low cost, the KRM-3Z7XXX is also suitable for integration in low to mid volume end-products. It is based on a Xilinx Zynq XC7Zxxx-xFxG676 SoC. The Xilinx SoC is accompanied by a 32 bit wide DDR3 memory subsystem on the PS and a 16 bit wide DDR3 memory on the PL, two instances of Quad SPI memory, power regulation, clock sources and 4 user LED.

The modules form-factor and pin assignment is fully compatible with the FOM7050 specification which defines the module outline of 50mm x 70mm x 11mm (with heat spreader), 21W maximum Module power, and the standard pin out.

Block diagram



Board dimensions

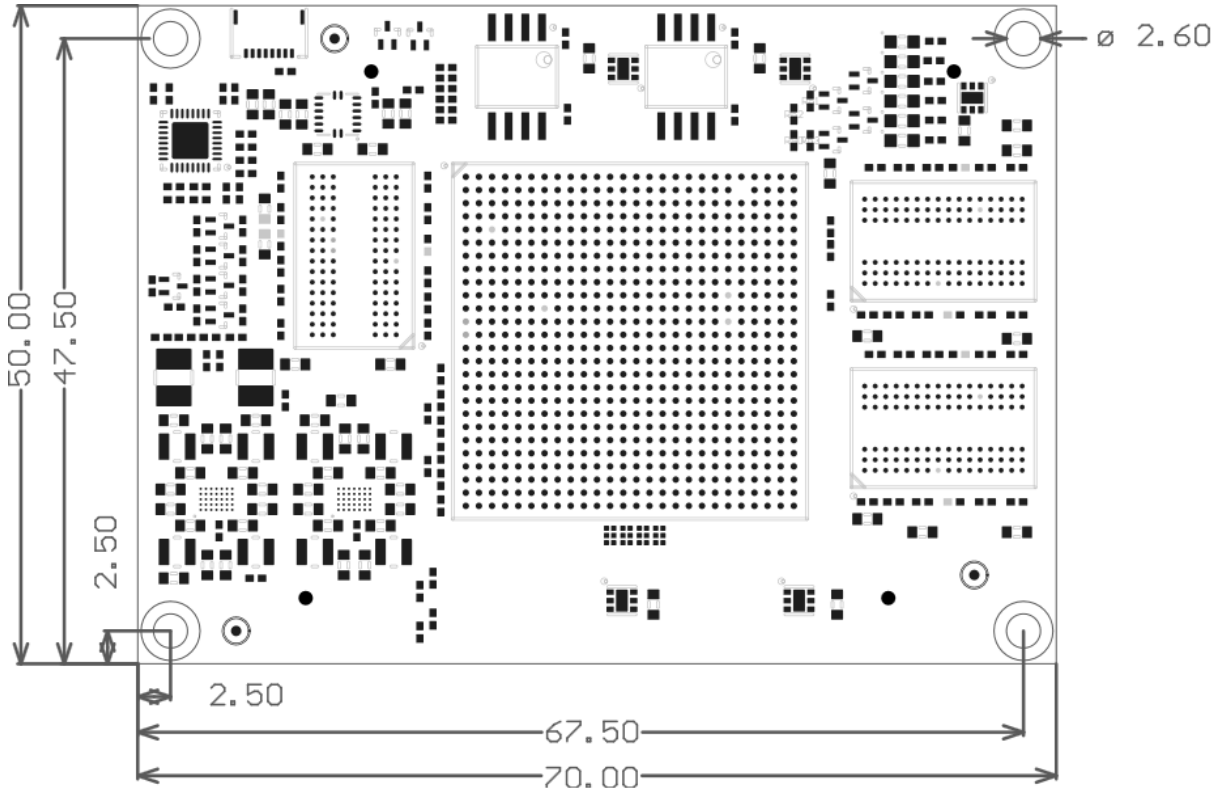


Figure 1: Board dimensions (in mm)

- Step Models of the module and its heat-spreader plate are available
- Altium PCB and Schematic templates are available

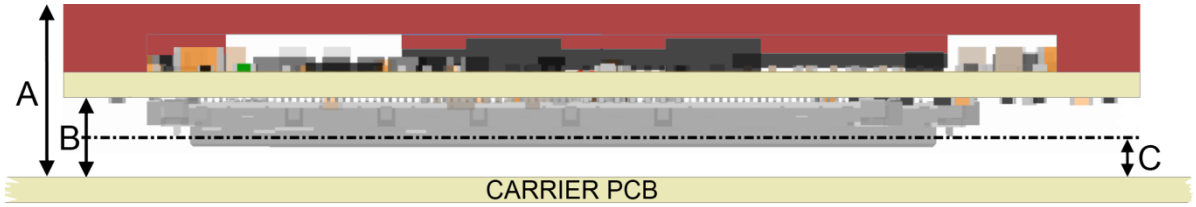


Figure 2: Board to board dimensions

- A = Height above carrier PCB ±0.2mm
- B = Mated stacking height
- C = Maximum component height area of carrier PCB.

Possible header variations:

– FX10A-168P-SV(85)	A = 10mm	B = 4mm	C = 1.5mm
– FX10A-168P-SV1(85)*	A = 11mm	B = 5mm	C = 2.5mm
– FX10A-168P-SV2(85)	A = 12mm	B = 6mm	C = 3.5mm
– FX10A-168P-SV3(85)	A = 13mm	B = 7mm	C = 4.5mm
– FX10A-168P-SV4(85)	A = 14mm	B = 8mm	C = 5.5mm

*KRC3701_CARRIER

Features

Overview

- Xilinx XC7Zxxx-xFxG676x[i]
  - Available in speed grades 1 through 3; Commercial or industrial temperature range as options
  - 78’600 to 218'600 LUTs
  - 157’200 to 437'400 Flip-Flops
  - 400 to 900 DSP Slices /18x25 MACCs
  - 265 to 545 x 36Kb block RAMs
  - Dual ARM A9 Cores with NEON co-processor
  - 256kB OC-RAM

- 1GB of LPDDR3 SDRAM PS memory
- 256MB of LPDDR3 SDRAM PL memory

- 256Mbit QUAD SPI; 2 times 128Mbit

- 2x 168 pin Hirose FX10 dual row connectors
  - 4x PL I/O bank (Banks 12, 13, 34, 35)
    - 48 pins each
    - All byte groups (0-3) intact and length matched
    - I/O voltage supplied by carrier board, can be different for each bank
    - External I/O Voltage is switched; switch is enabled by on-board PoK signal
  - 1x PS MIO1 bank
    - MIO 16 through 53 (all of bank 501)
    - 1V8 default, supplied by KRM on-board regulator
  - JTAG chain to FPGA; 3V3
  - Configuration OK; buffered open collector output

- 33.333 MHz on-board oscillator

- 4 User LED driven by bank 34 & 35 I/O_0 and I/O_25 (not part of byte groups on I/O connector)

- MGT: 4 lanes + 1 reference clock or 8 lanes + 2 reference clocks

[i] “x” will be replaced by version specific codes, please refer to “Module Configurations” towards the end of the datasheet for details and valid combinations

Power supply and power considerations

Core power

-The KRM-3Z7XXX requires a **stable** power supply of 3V3. In order to support designs with high FPGA utilization, a supply capable of providing at least 6A is required, 8A is recommended.
-Each of the 4 pin-groups of the 3V3 Global supply must be bypassed with a minimum of 47uF on the carrier board.
-Each Bank I/O supply must be bypassed with a minimum of 47uF on the carrier board.

I/O Bank Power sequence

I/O Bank power is to be supplied by the user design on the carrier board and may range from 1V35 to 3V3 for high-range banks or 1V35 to 1V8 for high-performance banks. Each I/O bank may be powered by a different I/O voltage, for maximum flexibility of the module.
In order to ensure optimal power sequencing of the power rails as recommended by Xilinx, the I/O Bank power is switched by on-board FET so that the user does not have to be concerned about the power sequencing of I/O voltages. The power-up of the I/O banks can be enabled by the "Pok" of the on board regulators or the "config-done" of the FPGA.
The default power on of the I/O power rails is driven by the signal that indicates the completion of the FPGA configuration.

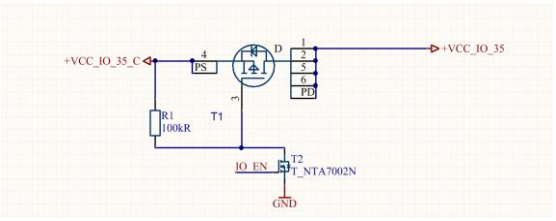


Figure 3

Supply Type	FX10 pin number	Voltage	Current	Remark
Global Module supply for internal regulators and CFG circuits	X1: 1,2, 165,166,167,168[i] X2: 1,2,3,4,165,166,167,168	3V3 Global	4.2A [ii]	Bypass each corner with at least 47uF on carrier
I/O Supply X1 GROUP1 (BANK 13)	X1:29,30	1V35 to 3V3	600mA [iii]	Bypass with at least 47uF on carrier
I/O Supply X1 GROUP2 (BANK 12)	X1:83,84	1V35 to 3V3	600mA	Bypass with at least 47uF on carrier
I/O Supply X2 GROUP1 (BANK 35)	X2: 31,32	1V35 to 1V8[iv]	600mA	Bypass with at least 47uF on carrier
I/O Supply X2 GROUP2 (BANK 34)	X2: 85,86	1V35 to 1V8[v]	600mA	Bypass with at least 47uF on carrier

[i] In order to ensure best performance with MGT capable modules, treat X1: 165-168 as low noise supply pins and isolate with a ferrite bead /capacitor Pi filter from other 3V3 rails.
[ii] The maximum core power to the Module is 14x 0.3A @3.3V = 13.86W.
[iii] The maximum I/O power to the module is 4x 0.6A @3.3V = 7.92W
[iv] Limit to 1V8 in order to ensure full compatibility with all modules of the KRM-3 series
[v] Limit to 1V8 in order to ensure full compatibility with all modules of the KRM-3 series

Clocking resources

Onboard oscillator

The onboard oscillator provides 33.33 MHz to the PS PLL of the SoC.

External PL Fabric clocks

Each bank exposes all clock capable pins, please consult the I/O tables and Xilinx clocking guide for details.

External MGT clocks

Two MGT clock inputs are provided through the FX10 connector interface, please consult the I/O tables.

Reset

-The PS reset port is available in the configuration and housekeeping signal group on connector X2: Pin115
-The reset pin is internally pulled up to 3V3 Global and forwarded to the PS reset pin via the BMC.
-Power-on-reset (PoR) is available via HW_RESET_IN on connector X2: Pin125.
-The module is kept in hardware reset until all voltages are stable.
-The module is self-resetting at power up, no external reset or power monitor is required or recommended.
-Unless there is an explicit need for a HW reset capability, tie pin X2:125 to GND.
-Reset_INn is best left unconnected or driven by an open drain source such as a JTAG adapter.

Signal name	FPGA pin	Board connector	Direction	Remark	I/O Level
RESET_INn	NA	X2: Pin115	FX10 → BMC ->FPGA	active low	INT PU to 3V3
HW_RESET_IN	NA	X2: Pin125	FX10 ->BMC -> FPGA	active high	3V3

Ready

-The module reports the conclusion of the configuration process via the signal CFG_OKn on connector X2:Pin116.
-CFG_OKn is a connected to a dedicated FET and implemented as an open drain output. It may sink as much as 50mA. An external pull-up resistor is required.
-CFG_OKn is provided by the BMC controller and derived from the Config-Done signal of the FPGA.
-CFG_OKn goes low after the FPGA/SoC has been configured successfully.

Signal name	FPGA pin	Board connector	Direction	Remark	I/O Level
CFG_OKn	NA	X2: Pin116	FPGA→ BMC -> FX10	active low	OC

VCCBATT_0

The VCCBATT_0 input is available via V_BATT_IN on connector X2: Pin126. Please consult the Xilinx datasheet for V-Batt requirement details. If not used, tie to GND.

Signal name	FPGA pin	Board connector	Direction	Remark	I/O Level
V_BATT_IN	V15	X2: Pin126	X2 -> FPGA	active high	2V max

Configuration

JTAG Interface

The FPGA configuration file - i.e. the FPGA firmware - can be loaded via dedicated JTAG pins

	Signal name	Board connector	Direction	Remark	I/O Level
JTAG	TMS	X2:118	FX10 → FPGA		3V3
	TCK	X2:117	FX10 → FPGA		3V3
	TDO	X2:120	FPGA → FX10		3V3
	TDI	X2:119	FX10 → FPGA		3V3

Mode Pins

The MIO_0 Bank of the PS system (Bank 500) is not exposed on the modules I/O pins but dedicated to the modules internal functions such as configuration and housekeeping.
Mode pins MIO_02 through MIO_08 are largely dual-use; they determine the power-up-mode and are also used to implement the two QSPI interfaces.

The pin MIO_07 is used to set the MIO Bank0 to 3.3V. The pin MIO_08 is used to set the MIO Bank1 to 1.8V. A Board management Controller (BMC) is used to determine the Boot Source (SD-Card or QSPI), the Boot Mode (JTAG or Self) and to enable the PLL. By default, the Boot Source is set to SD-Card and the Boot Mode to Self. Thus, on power up, the system will boot automatically from the SD-Card of the carrier.

It is possible to modify the Boot Source and the Boot Mode by sending the appropriate commands to the BMC through a serial connection. Please, refer to the document entitled *BMC_how_to_guide.pdf* for more information.

On-Board Quad SPI Configuration Memory

Two instances of QSPI memory are implemented on the module.

Each instance is populated with a 128Mbit QSPI flash.

	Signal name	MIO	Direction	Remark	I/O Level
QSPI0	S#	MIO_01	FPGA → SPI	Pull up on Module	3V3
	DQ0	MIO_02	BI-DIR		3V3
	DQ1	MIO_03	BI-DIR		3V3
	DQ2/W#	MIO_04	BI-DIR		3V3
	DQ3/HOLD#	MIO_05	BI-DIR		3V3
	CLK	MIO_06	FPGA → SPI		3V3

	Signal name	MIO	Direction	Remark	I/O Level
QSPI1	S#	MIO_00	FPGA → SPI	Pull up on Module	3V3
	DQ0	MIO_10	BI-DIR		3V3
	DQ1	MIO_11	BI-DIR		3V3
	DQ2/W#	MIO_12	BI-DIR		3V3
	DQ3/HOLD#	MIO_13	BI-DIR		3V3
	CLK	MIO_09	FPGA → SPI		3V3

DDR3 SDRAM

-The KRM-3Z7XXX PS memory is populated with two DDR3 SDRAM providing a total of 8Gb of RAM, organized as 256M x 32 bit (1GB).
-The Memory subsystem can run as fast as 1066MT/s even on the slowest speed grade SoC.
-The KRM-3Z7XXX implementation takes advantage of the lower power requirements of 1.35V operation.

-The KRM-3Z7XXX PL Memory is populated with one DDR3 SDRAM providing a total of 2Gb of RAM, organized as 128M x 16 bit (256MB). As of Board revision E, the PL Ram supports byte masking and is therefore compatible with an AXI connected memory interface. Please consult the migration guide for differences in PL memory connectivity of previous board Revisions.
-The PL Memory subsystem can run as fast as 1333MT/s even on the slowest speed grade SoC with the VAUX_IO set to 2V0. If lower memory performance is sufficient, the VAUX_IO may be set to 1V8 for a maximum performance of 800 MT/s at lower power consumption.

A reference design based on the Xilinx MIG core is available to demonstrate the performance of the PL DDR3 memory of the module. For more information, refer to the document "*PL_DDR3_MIG_Controller_tutorial.pdf*".

I/O Headers

The KRM-3Z7XXX s I/O pinning is fully compatible all future releases of KRM-3 series modules
Two Hirose FX10 168 pin connectors provide a total of 192 PL I/O signals, 38 PS MIO signals, 4MGT lanes, 1 differential MGT reference clocks, configuration and status pins.
Matching connectors for the carrier board design are:

- FX10A-168P-SVx

Please note HIROSE annotation is Pin **1a to 84a** and **1b to 84b**
This corresponds to KR annotation Pin **1 to 167** and **2 to 168**

	Group	FPGA Bank	Remark	I/O Level
X1	X1_1	Bank 13	3V3 or below high range	3V3 to 1V35
	X1_2	Bank 12	3V3 or below high range	3V3 to 1V35
	X1_MGT	x8		

	Group	FPGA Bank	Remark	I/O Level
X2	X2_1	Bank 35	1V8 MAX high performance	1V8 to 1V35
	X2_2	Bank 34	1V8 MAX high performance	1V8 to 1V35
	X2_CFG	CFG		3V3
	X2_MIO	MIO_1/501	1V8	1V8

PL BANKS

- The Byte-groups of a PL I/O bank (T0 –T3) are kept as a group and are length matched on the module.
- Differential I/O capable pins of the PL are routed as coupled differential pairs.

The I/O headers X1 and X2 feature I/O groups that are the same on all KRM-3Z7xxx modules. The I/O groups are the same for each module of the KRM-3Z7xxx family but each module may map different ports to the I/O groups. In order to be fully compatible with all currently planned KRM-3Z7xxx compliant modules, the X2 I/O banks should only use I/O voltages of 1V8 or less as some Modules map **High performance** banks instead of **High range** banks onto X2.

The I/O banks on X2 of the KRM-3Z7xxx module are High performance banks and may only use supply voltages up to 1V8.

MIO BANK

The MIO Bank I/O voltage is 1V8. **Only** 1V8 MIO supply is supported on KRC carriers.
MIO signals 16 through 53 (Bank 501) are available. In order to be compatible with KR issued Linux BSP's we recommend using the MIO assignment as shown on one of the KR issued Evaluation boards such as the KRC3701 carrier. Naturally other configurations are possible, contact KR for BSP support of your desired configuration.

MGT BANK

All 4 or 8 MGT lanes are available on the MGT block of X1. One external reference clock(s) may be applied so that the module can simultaneously support MGT standards that are based on one or two different clock reference. The clock signals are DC coupled on the module and require AC coupling on the carrier.
All MGT TX signal pairs are AC coupled on the module; no capacitors are required on the carrier board.

Connector Schematic

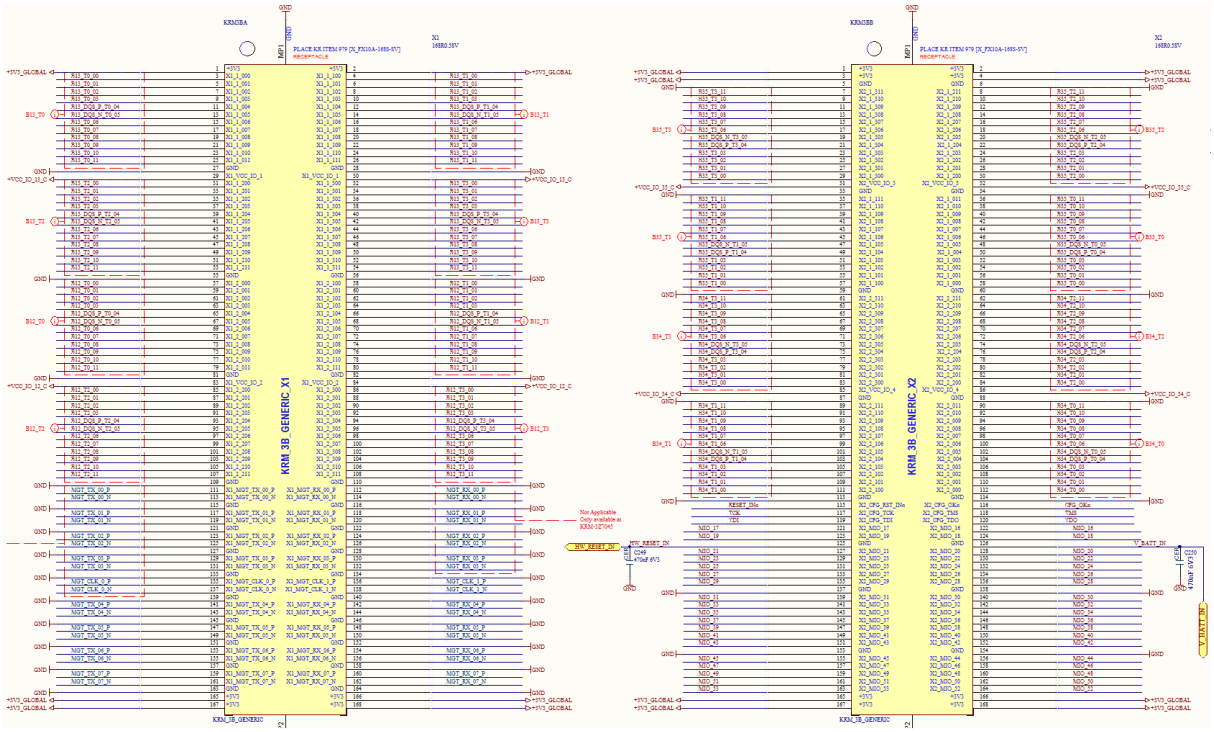


Figure 4

Pin Mapping

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
NA	**NA**	R13	DXN_0	NA	0	CONFIG		NA	NC
VCCADC_0	**NA**	M14	VCCADC_0	NA	0	CONFIG		VCC_AUX_PL_PS	+1V8
GNDADC_0	**NA**	M13	GNDADC_0	NA	0	CONFIG		GND	GND
NA	**NA**	R14	DXP_0	NA	0	CONFIG		NA	NC
NA	**NA**	N13	VREFN_0	NA	0	CONFIG		NA	GND
NA	**NA**	P14	VREFP_0	NA	0	CONFIG		NA	GND
NA	**NA**	N14	VP_0	NA	0	CONFIG		NA	GND
NA	**NA**	P13	VN_0	NA	0	CONFIG		NA	GND
NA	**NA**	V15	VCCBATT_0	NA	0	CONFIG		NA	GND
RSVDGND	**NA**	V13	RSVDGND	NA	0	CONFIG		GND	GND
JTAG	**X2:117**	W12	TCK_0	NA	0	CONFIG	X2_CFG	+3V3_GLOBAL	
JTAG	**X2:118**	W11	TMS_0	NA	0	CONFIG	X2_CFG	+3V3_GLOBAL	
JTAG	**X2:119**	V11	TDI_0	NA	0	CONFIG	X2_CFG	+3V3_GLOBAL	
JTAG	**X2:120**	W10	TDO_0	NA	0	CONFIG	X2_CFG	+3V3_GLOBAL	
NA	**NA**	R8	INIT_B_0	NA	0	CONFIG		VCC_0_MIO0	+3V3
NA	**NA**	V9	PROGRAM_B_0	NA	0	CONFIG		VCC_0_MIO0	+3V3
NA	**NA**	T7	CFGBVS_0	NA	0	CONFIG		VCC_0_MIO0	+3V3
CFG_OK	**X2:116**	W9	DONE_0	NA	0	CONFIG	X2_CFG	VCC_0_MIO0	CFG_OKn after FET
NA	**NA**	W8	RSVDVCC1	NA	0	CONFIG		VCC_0_MIO0	+3V3
NA	**NA**	U8	RSVDVCC3	NA	0	CONFIG		VCC_0_MIO0	+3V3
NA	**NA**	V8	RSVDVCC2	NA	0	CONFIG		VCC_0_MIO0	+3V3
NA	**NA**	W14	IO_0_12	NA	12	HR	OB_SPARE	VIO_X1_2	NOT USED
PL_IO	**X1:57**	Y12	IO_L1P_T0_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:59**	Y11	IO_L1N_T0_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:61**	AB12	IO_L2P_T0_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:63**	AC11	IO_L2N_T0_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:65**	Y10	IO_L3P_T0_DQS_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:67**	AA10	IO_L3N_T0_DQS_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:69**	AB11	IO_L4P_T0_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:71**	AB10	IO_L4N_T0_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:73**	W13	IO_L5P_T0_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:75**	Y13	IO_L5N_T0_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:77**	AA13	IO_L6P_T0_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:79**	AA12	IO_L6N_T0_VREF_12	0	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:58**	AE10	IO_L7P_T1_12	1	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:60**	AD10	IO_L7N_T1_12	1	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:62**	AE12	IO_L8P_T1_12	1	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:64**	AF12	IO_L8N_T1_12	1	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:66**	AE11	IO_L9P_T1_DQS_12	1	12	HR	X1_2	VIO_X1_2	

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	**X1:68**	AF10	IO_L9N_T1_DQS_12	1	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:70**	AE13	IO_L10P_T1_12	1	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:72**	AF13	IO_L10N_T1_12	1	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:74**	AC12	IO_L11P_T1_SRCC_12	1	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:76**	AD11	IO_L11N_T1_SRCC_12	1	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:78**	AC13	IO_L12P_T1_MRCC_12	1	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:80**	AD13	IO_L12N_T1_MRCC_12	1	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:85**	AC14	IO_L13P_T2_MRCC_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:87**	AD14	IO_L13N_T2_MRCC_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:89**	AB15	IO_L14P_T2_SRCC_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:91**	AB14	IO_L14N_T2_SRCC_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:93**	AD16	IO_L15P_T2_DQS_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:95**	AD15	IO_L15N_T2_DQS_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:97**	AF15	IO_L16P_T2_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:99**	AF14	IO_L16N_T2_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:101**	AE16	IO_L17P_T2_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:103**	AE15	IO_L17N_T2_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:105**	AE17	IO_L18P_T2_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:107**	AF17	IO_L18N_T2_12	2	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:86**	Y17	IO_L19P_T3_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:88**	AA17	IO_L19N_T3_VREF_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:90**	AB17	IO_L20P_T3_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:92**	AB16	IO_L20N_T3_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:94**	AC17	IO_L21P_T3_DQS_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:96**	AC16	IO_L21N_T3_DQS_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:98**	AA15	IO_L22P_T3_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:100**	AA14	IO_L22N_T3_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:102**	Y16	IO_L23P_T3_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:104**	Y15	IO_L23N_T3_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:106**	W16	IO_L24P_T3_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**X1:108**	W15	IO_L24N_T3_12	3	12	HR	X1_2	VIO_X1_2	
PL_IO	**NA**	W17	IO_25_12	NA	12	HR	OB_SPARE	VIO_X1_2	NOT USED
PL_IO	**NA**	V19	IO_0_13	NA	13	HR	OB_SPARE	VIO_X1_1	NOT USED
PL_IO	**X1:3**	AA25	IO_L1P_T0_13	0	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:5**	AB25	IO_L1N_T0_13	0	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:7**	AB26	IO_L2P_T0_13	0	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:9**	AC26	IO_L2N_T0_13	0	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:11**	AE25	IO_L3P_T0_DQS_13	0	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:13**	AE26	IO_L3N_T0_DQS_13	0	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:15**	AD25	IO_L4P_T0_13	0	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:17**	AD26	IO_L4N_T0_13	0	13	HR	X1_1	VIO_X1_1	

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	**X1:19**	AF24	IO_L5P_T0_13	0	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:21**	AF25	IO_L5N_T0_13	0	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:23**	AA24	IO_L6P_T0_13	0	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:25**	AB24	IO_L6N_T0_VREF_13	0	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:4**	AE22	IO_L7P_T1_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:6**	AF22	IO_L7N_T1_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:8**	AE23	IO_L8P_T1_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:10**	AF23	IO_L8N_T1_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:12**	AB21	IO_L9P_T1_DQS_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:14**	AB22	IO_L9N_T1_DQS_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:16**	AA22	IO_L10P_T1_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:18**	AA23	IO_L10N_T1_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:20**	AD23	IO_L11P_T1_SRCC_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:22**	AD24	IO_L11N_T1_SRCC_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:24**	AC23	IO_L12P_T1_MRCC_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:26**	AC24	IO_L12N_T1_MRCC_13	1	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:31**	AD20	IO_L13P_T2_MRCC_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:33**	AD21	IO_L13N_T2_MRCC_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:35**	AC21	IO_L14P_T2_SRCC_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:37**	AC22	IO_L14N_T2_SRCC_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:39**	AF19	IO_L15P_T2_DQS_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:41**	AF20	IO_L15N_T2_DQS_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:43**	AE20	IO_L16P_T2_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:45**	AE21	IO_L16N_T2_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:47**	AD18	IO_L17P_T2_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:49**	AD19	IO_L17N_T2_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:51**	AE18	IO_L18P_T2_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:53**	AF18	IO_L18N_T2_13	2	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:32**	W20	IO_L19P_T3_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:34**	Y20	IO_L19N_T3_VREF_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:36**	AA20	IO_L20P_T3_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:38**	AB20	IO_L20N_T3_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:40**	AC18	IO_L21P_T3_DQS_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:42**	AC19	IO_L21N_T3_DQS_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:44**	AA19	IO_L22P_T3_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:46**	AB19	IO_L22N_T3_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:48**	W18	IO_L23P_T3_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:50**	W19	IO_L23N_T3_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:52**	Y18	IO_L24P_T3_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**X1:54**	AA18	IO_L24N_T3_13	3	13	HR	X1_1	VIO_X1_1	
PL_IO	**NA**	V18	IO_25_13	NA	13	HR	OB_SPARE	VIO_X1_1	NOT USED

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_VRN	NA	L9	IO_0_VRN_33	NA	33	HP	NA	VCCO_DDR	PULL UP
PL_RAM	NA	G4	IO_L1P_T0_33	0	33	HP	NA	VCCO_DDR	U14_DQ4
PL_RAM	NA	F4	IO_L1N_T0_33	0	33	HP	NA	VCCO_DDR	U14_DQ5
PL_RAM	NA	D4	IO_L2P_T0_33	0	33	HP	NA	VCCO_DDR	U14_DQ1
PL_RAM	NA	D3	IO_L2N_T0_33	0	33	HP	NA	VCCO_DDR	U14_DQ7
PL_RAM	NA	G2	IO_L3P_T0_DQS_33	0	33	HP	NA	VCCO_DDR	U14_LDQS_P
PL_RAM	NA	F2	IO_L3N_T0_DQS_33	0	33	HP	NA	VCCO_DDR	U14_LDQS_N
PL_RAM	NA	D1	IO_L4P_T0_33	0	33	HP	NA	VCCO_DDR	U14_DQ0
PL_RAM	NA	C1	IO_L4N_T0_33	0	33	HP	NA	VCCO_DDR	U14_DQ6
PL_RAM	NA	E2	IO_L5P_T0_33	0	33	HP	NA	VCCO_DDR	U14_DQ3
PL_RAM	NA	E1	IO_L5N_T0_33	0	33	HP	NA	VCCO_DDR	U14_DQ2
NA	NA	F3	IO_L6P_T0_33	0	33	HP	NA	VCCO_DDR	NA
PL_VREF	NA	E3	IO_L6N_T0_VREF_33	0	33	HP	NA	VREF	+0V625
PL_RAM	NA	J1	IO_L7P_T1_33	1	33	HP	NA	VCCO_DDR	U14_A0
PL_RAM	NA	H1	IO_L7N_T1_33	1	33	HP	NA	VCCO_DDR	U14_A2
PL_RAM	NA	H4	IO_L8P_T1_33	1	33	HP	NA	VCCO_DDR	U14_A13
PL_RAM	NA	H3	IO_L8N_T1_33	1	33	HP	NA	VCCO_DDR	U14_A11
PL_RAM	NA	K2	IO_L9P_T1_DQS_33	1	33	HP	NA	VCCO_DDR	U14_BA0
PL_RAM	NA	K1	IO_L9N_T1_DQS_33	1	33	HP	NA	VCCO_DDR	U14_A4
PL_RAM	NA	H2	IO_L10P_T1_33	1	33	HP	NA	VCCO_DDR	U14_A7
PL_RAM	NA	G1	IO_L10N_T1_33	1	33	HP	NA	VCCO_DDR	U14_A9
PL_RAM	NA	L3	IO_L11P_T1_SRCC_33	1	33	HP	NA	VCCO_DDR	U14_ODT
PL_RAM	NA	K3	IO_L11N_T1_SRCC_33	1	33	HP	NA	VCCO_DDR	U14_A1
PL_RAM	NA	J4	IO_L12P_T1_MRCC_33	1	33	HP	NA	VCCO_DDR	U14_A8
PL_RAM	NA	J3	IO_L12N_T1_MRCC_33	1	33	HP	NA	VCCO_DDR	U14_A6
PL_RAM	NA	M6	IO_L13P_T2_MRCC_33	2	33	HP	NA	VCCO_DDR	U14_BA2
PL_RAM	NA	M5	IO_L13N_T2_MRCC_33	2	33	HP	NA	VCCO_DDR	U14_BA1
PL_RAM	NA	L5	IO_L14P_T2_SRCC_33	2	33	HP	NA	VCCO_DDR	U14_A5
PL_RAM	NA	L4	IO_L14N_T2_SRCC_33	2	33	HP	NA	VCCO_DDR	U14_A3
PL_RAM	NA	N3	IO_L15P_T2_DQS_33	2	33	HP	NA	VCCO_DDR	U14_RAS_B
PL_RAM	NA	N2	IO_L15N_T2_DQS_33	2	33	HP	NA	VCCO_DDR	U14_CKE
PL_RAM	NA	M2	IO_L16P_T2_33	2	33	HP	NA	VCCO_DDR	U14_A10
PL_RAM	NA	L2	IO_L16N_T2_33	2	33	HP	NA	VCCO_DDR	U14_A12
PL_RAM	NA	N4	IO_L17P_T2_33	2	33	HP	NA	VCCO_DDR	U14_CAS_B
PL_RAM	NA	M4	IO_L17N_T2_33	2	33	HP	NA	VCCO_DDR	U14_WE_B
PL_RAM	NA	N1	IO_L18P_T2_33	2	33	HP	NA	VCCO_DDR	U14_CK_P
PL_RAM	NA	M1	IO_L18N_T2_33	2	33	HP	NA	VCCO_DDR	U14_CK_N
PL_RAM	NA	M7	IO_L19P_T3_33	3	33	HP	NA	VCCO_DDR	U14_RESET_B
PL_VREF	NA	L7	IO_L19N_T3_VREF_33	3	33	HP	NA	VREF	+0V75
PL_RAM	NA	K5	IO_L20P_T3_33	3	33	HP	NA	VCCO_DDR	U14_DQ13
PL_RAM	NA	J5	IO_L20N_T3_33	3	33	HP	NA	VCCO_DDR	U14_DQ8

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_RAM	NA	M8	IO_L21P_T3_DQS_33	3	33	HP	NA	VCCO_DDR	U14_UDQS_P
PL_RAM	NA	L8	IO_L21N_T3_DQS_33	3	33	HP	NA	VCCO_DDR	U14_UDQS_N
PL_RAM	NA	K6	IO_L22P_T3_33	3	33	HP	NA	VCCO_DDR	U14_DQ14
PL_RAM	NA	J6	IO_L22N_T3_33	3	33	HP	NA	VCCO_DDR	U14_DQ10
PL_RAM	NA	N7	IO_L23P_T3_33	3	33	HP	NA	VCCO_DDR	U14_DQ11
PL_RAM	NA	N6	IO_L23N_T3_33	3	33	HP	NA	VCCO_DDR	U14_DQ15
PL_RAM	NA	K8	IO_L24P_T3_33	3	33	HP	NA	VCCO_DDR	U14_DQ9
PL_RAM	NA	K7	IO_L24N_T3_33	3	33	HP	NA	VCCO_DDR	U14_DQ12
PL_VRP	NA	N8	IO_25_VRP_33	NA	33	HP	NA	GND	PULL DOWN
LED_2	NA	H16	IO_0_VRN_35	NA	35	HP	OB_LED	VIO_X2_1	USR_LED_2
PL_IO	**X2:58**	F12	IO_L1P_T0_AD0P_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:56**	E12	IO_L1N_T0_AD0N_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:54**	E10	IO_L2P_T0_AD8P_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:52**	D10	IO_L2N_T0_AD8N_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:50**	G10	IO_L3P_T0_DQS_AD1P_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:48**	F10	IO_L3N_T0_DQS_AD1N_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:46**	E11	IO_L4P_T0_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:44**	D11	IO_L4N_T0_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:42**	G12	IO_L5P_T0_AD9P_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:40**	G11	IO_L5N_T0_AD9N_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:38**	F13	IO_L6P_T0_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:36**	E13	IO_L6N_T0_VREF_35	0	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:57**	H13	IO_L7P_T1_AD2P_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:55**	H12	IO_L7N_T1_AD2N_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:53**	K13	IO_L8P_T1_AD10P_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:51**	J13	IO_L8N_T1_AD10N_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:49**	K15	IO_L9P_T1_DQS_AD3P_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:47**	J15	IO_L9N_T1_DQS_AD3N_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:45**	G16	IO_L10P_T1_AD11P_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:43**	G15	IO_L10N_T1_AD11N_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:41**	G14	IO_L11P_T1_SRCC_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:39**	F14	IO_L11N_T1_SRCC_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:37**	J14	IO_L12P_T1_MRCC_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:35**	H14	IO_L12N_T1_MRCC_35	1	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:30**	D15	IO_L13P_T2_MRCC_35	2	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:28**	D14	IO_L13N_T2_MRCC_35	2	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:26**	F15	IO_L14P_T2_AD4P_SRCC_35	2	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:24**	E15	IO_L14N_T2_AD4N_SRCC_35	2	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:22**	C17	IO_L15P_T2_DQS_AD12P_35	2	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:20**	C16	IO_L15N_T2_DQS_AD12N_35	2	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:18**	E16	IO_L16P_T2_35	2	35	HP	X2_1	VIO_X2_1	

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	**X2:16**	D16	IO_L16N_T2_35	2	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:14**	B16	IO_L17P_T2_AD5P_35	2	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:12**	B15	IO_L17N_T2_AD5N_35	2	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:10**	B17	IO_L18P_T2_AD13P_35	2	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:8**	A17	IO_L18N_T2_AD13N_35	2	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:29**	D13	IO_L19P_T3_35	3	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:27**	C13	IO_L19N_T3_VREF_35	3	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:25**	C14	IO_L20P_T3_AD6P_35	3	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:23**	B14	IO_L20N_T3_AD6N_35	3	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:21**	A15	IO_L21P_T3_DQS_AD14P_35	3	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:19**	A14	IO_L21N_T3_DQS_AD14N_35	3	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:17**	C12	IO_L22P_T3_AD7P_35	3	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:15**	B12	IO_L22N_T3_AD7N_35	3	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:13**	C11	IO_L23P_T3_35	3	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:11**	B11	IO_L23N_T3_35	3	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:9**	A13	IO_L24P_T3_AD15P_35	3	35	HP	X2_1	VIO_X2_1	
PL_IO	**X2:7**	A12	IO_L24N_T3_AD15N_35	3	35	HP	X2_1	VIO_X2_1	
LED_1	NA	K12	IO_25_VRP_35	NA	35	HP	OB_LED	VIO_X2_1	USR_LED_1
LED_4	NA	K11	IO_0_VRN_34	NA	34	HP	OB_LED	VIO_X2_2	USR_LED_4
PL_IO	**X2:112**	J11	IO_L1P_T0_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:110**	H11	IO_L1N_T0_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:108**	G6	IO_L2P_T0_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:106**	G5	IO_L2N_T0_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:104**	H9	IO_L3P_T0_DQS_PUDC_B_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:102**	G9	IO_L3N_T0_DQS_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:100**	H7	IO_L4P_T0_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:98**	H6	IO_L4N_T0_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:96**	J10	IO_L5P_T0_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:94**	J9	IO_L5N_T0_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:92**	J8	IO_L6P_T0_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:90**	H8	IO_L6N_T0_VREF_34	0	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:111**	F5	IO_L7P_T1_34	1	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:109**	E5	IO_L7N_T1_34	1	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:107**	D9	IO_L8P_T1_34	1	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:105**	D8	IO_L8N_T1_34	1	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:103**	F9	IO_L9P_T1_DQS_34	1	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:101**	E8	IO_L9N_T1_DQS_34	1	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:99**	E6	IO_L10P_T1_34	1	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:97**	D5	IO_L10N_T1_34	1	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:95**	F8	IO_L11P_T1_SRCC_34	1	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:93**	E7	IO_L11N_T1_SRCC_34	1	34	HP	X2_2	VIO_X2_2	

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PL_IO	**X2:91**	G7	IO_L12P_T1_MRCC_34	1	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:89**	F7	IO_L12N_T1_MRCC_34	1	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:84**	C8	IO_L13P_T2_MRCC_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:82**	C7	IO_L13N_T2_MRCC_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:80**	D6	IO_L14P_T2_SRCC_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:78**	C6	IO_L14N_T2_SRCC_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:76**	C9	IO_L15P_T2_DQS_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:74**	B9	IO_L15N_T2_DQS_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:72**	B10	IO_L16P_T2_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:70**	A10	IO_L16N_T2_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:68**	A9	IO_L17P_T2_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:66**	A8	IO_L17N_T2_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:64**	B7	IO_L18P_T2_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:62**	A7	IO_L18N_T2_34	2	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:83**	C4	IO_L19P_T3_34	3	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:81**	C3	IO_L19N_T3_VREF_34	3	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:79**	B5	IO_L20P_T3_34	3	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:77**	B4	IO_L20N_T3_34	3	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:75**	B6	IO_L21P_T3_DQS_34	3	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:73**	A5	IO_L21N_T3_DQS_34	3	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:71**	A4	IO_L22P_T3_34	3	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:69**	A3	IO_L22N_T3_34	3	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:67**	C2	IO_L23P_T3_34	3	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:65**	B1	IO_L23N_T3_34	3	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:63**	B2	IO_L24P_T3_34	3	34	HP	X2_2	VIO_X2_2	
PL_IO	**X2:61**	A2	IO_L24N_T3_34	3	34	HP	X2_2	VIO_X2_2	
LED_3	NA	K10	IO_25_VRP_34	NA	34	HP	OB_LED	VIO_X2_2	USR_LED_3
MGT	**X1:111**	AF8	MGTXTXP0_111	NA	111	GTX	X1_MGT	MGTAV	Only 035/045
MGT	**X1:112**	AD8	MGTXRXP0_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:113**	AF7	MGTXTXN0_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:114**	AD7	MGTXRXN0_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:117**	AF4	MGTXTXP1_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:118**	AE6	MGTXRXP1_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:119**	AF3	MGTXTXN1_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:120**	AE5	MGTXRXN1_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:123**	AE2	MGTXTXP2_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:124**	AC6	MGTXRXP2_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:125**	AE1	MGTXTXN2_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:126**	AC5	MGTXRXN2_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:129**	AC2	MGTXTXP3_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:130**	AD4	MGTXRXP3_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
MGT	**X1:131**	AC1	MGTXTXN3_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:132**	AD3	MGTXRXN3_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:135**	W6	MGTREFCLK0P_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:136**	R6	MGTREFCLK0P_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:137**	W5	MGTREFCLK0N_111	NA	111	GTX	X1:MGT	MGTAV	Only 035/045
MGT	**X1:138**	R5	MGTREFCLK0N_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:141**	AA2	MGTXTXP0_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:142**	AB4	MGTXRXP0_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:143**	AA1	MGTXTXN0_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:144**	AB3	MGTXRXN0_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:147**	W2	MGTXTXP1_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:148**	Y4	MGTXRXP1_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:149**	W1	MGTXTXN1_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:150**	Y3	MGTXRXN1_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:153**	U2	MGTXTXP2_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:154**	V4	MGTXRXP2_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:155**	U1	MGTXTXN2_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:156**	V3	MGTXRXN2_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:159**	R2	MGTXTXP3_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:160**	T4	MGTXRXP3_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:161**	R1	MGTXTXN3_112	NA	112	GTX	X1:MGT	MGTAV	All variants
MGT	**X1:162**	T3	MGTXRXN3_112	NA	112	GTX	X1:MGT	MGTAV	All variants
NA	NA	AA5	NA	NA	NA	NA	NA	MGTAV	
NA	NA	AA6	NA	NA	NA	NA	NA	MGTAV	
NA	NA	U5	MGTREFCLK1N_112	NA	112	GTX	NA	MGTAV	
NA	NA	U6	MGTREFCLK1P_112	NA	112	GTX	NA	MGTAV	
INT_REF	NA	AB7	MGTAVTTRCAL_112	NA	112	GTX	NA	MGTAVTT	
INT_REF	NA	AB8	MGTRREF_112	NA	112	GTX	NA	MGTAVTT	
POR	NA	C23	PS_POR_B_500	NA	500	MIO	OB_INT	+3V3_GLOBAL	Intern P_OK
CLK_IN	NA	B24	PS_CLK_500	NA	500	MIO	OB_INT	+3V3_GLOBAL	33MHZ
CFG	NA	E26	PS_MIO0_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_S#
CFG	NA	D26	PS_MIO1_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_S#
CFG_MODE	NA	E25	PS_MIO2_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_DQ0
CFG_MODE	NA	D25	PS_MIO3_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_DQ1
CFG_MODE	NA	F24	PS_MIO4_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_DQ2
CFG_MODE	NA	C26	PS_MIO5_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_DQ3
CFG_MODE	NA	F23	PS_MIO6_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U10_CLK
CFG_MODE	NA	E23	PS_MIO7_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	MODE_PIN
CFG_MODE	NA	A24	PS_MIO8_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	MODE_PIN
CFG	NA	D24	PS_MIO9_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_CLK
CFG	NA	A25	PS_MIO10_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_DQ0

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
CFG	NA	B26	PS_MIO11_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_DQ1
CFG	NA	A23	PS_MIO12_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_DQ2
CFG	NA	B25	PS_MIO13_500	NA	500	MIO	OB_MIO	+3V3_GLOBAL	U11_DQ3
NA	NA	D23	PS_MIO14_500	NA	500	MIO	OB_MIO	NA	
NA	NA	C24	PS_MIO15_500	NA	500	MIO	OB_MIO	NA	
VREF	NA	H18	PS_MIO_VREF_501	NA	501	MIO	OB_P	VCC_MIO1	
PS_IO	**X2:121**	G17	PS_MIO17_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:123**	G19	PS_MIO19_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:127**	F22	PS_MIO21_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:129**	F20	PS_MIO23_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:131**	F19	PS_MIO25_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:133**	F18	PS_MIO27_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:135**	E20	PS_MIO29_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:139**	E21	PS_MIO31_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:141**	E22	PS_MIO33_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:143**	D19	PS_MIO35_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:148**	D21	PS_MIO38_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:150**	C22	PS_MIO40_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:152**	F17	PS_MIO42_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:156**	E18	PS_MIO44_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:158**	E17	PS_MIO46_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:160**	B21	PS_MIO48_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:162**	B22	PS_MIO50_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:164**	A20	PS_MIO52_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_RST	**X2:115**	A22	PS_SRST_B_501	NA	501	MIO	X2_MIO	Int PU	Ext OC/OD
PS_IO	**X2:122**	G21	PS_MIO16_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:124**	G20	PS_MIO18_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:128**	H19	PS_MIO20_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:130**	G22	PS_MIO22_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:132**	J19	PS_MIO24_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:134**	H17	PS_MIO26_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:136**	J18	PS_MIO28_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:140**	K19	PS_MIO30_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:142**	K17	PS_MIO32_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:144**	J16	PS_MIO34_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:146**	K16	PS_MIO36_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:145**	D20	PS_MIO37_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:147**	C21	PS_MIO39_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:149**	C19	PS_MIO41_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:151**	D18	PS_MIO43_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:155**	C18	PS_MIO45_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PS_IO	**X2:157**	B19	PS_MIO47_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:159**	A18	PS_MIO49_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:161**	B20	PS_MIO51_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_IO	**X2:163**	A19	PS_MIO53_501	NA	501	MIO	X2_MIO	1V8_OB	+1V8
PS_RAM	NA	H22	PS_DDR_DRST_B_502	NA	502	DDR	NA	VCCO_DDR	RAM_RESET
PS_RAM	NA	F25	PS_DDR_DQ1_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ6
PS_RAM	NA	J26	PS_DDR_DQ0_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ4
PS_RAM	NA	G26	PS_DDR_DQ3_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ0
PS_RAM	NA	J25	PS_DDR_DQ2_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ2
PS_RAM	NA	G24	PS_DDR_DM0_502	NA	502	DDR	NA	VCCO_DDR	U15_LDM
PS_RAM	NA	G25	PS_DDR_DQS_N0_502	NA	502	DDR	NA	VCCO_DDR	U15_LDQS_N
PS_RAM	NA	H24	PS_DDR_DQS_P0_502	NA	502	DDR	NA	VCCO_DDR	U15_LDQS_P
PS_RAM	NA	H23	PS_DDR_DQ5_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ1
PS_RAM	NA	H26	PS_DDR_DQ4_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ3
PS_RAM	NA	J23	PS_DDR_DQ7_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ7
PS_RAM	NA	J24	PS_DDR_DQ6_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ5
PS_RAM	NA	L23	PS_DDR_DQ9_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ9
PS_RAM	NA	K26	PS_DDR_DQ8_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ11
PS_RAM	NA	K23	PS_DDR_DQ11_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ12
PS_RAM	NA	M26	PS_DDR_DQ10_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ8
PS_RAM	NA	K25	PS_DDR_DM1_502	NA	502	DDR	NA	VCCO_DDR	U15_UDM
PS_RAM	NA	L25	PS_DDR_DQS_N1_502	NA	502	DDR	NA	VCCO_DDR	U15_UDQS_N
PS_RAM	NA	L24	PS_DDR_DQS_P1_502	NA	502	DDR	NA	VCCO_DDR	U15_UDQS_P
PS_RAM	NA	N24	PS_DDR_DQ13_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ10
PS_RAM	NA	M25	PS_DDR_DQ12_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ15
PS_RAM	NA	N23	PS_DDR_DQ15_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ13
PS_RAM	NA	M24	PS_DDR_DQ14_502	NA	502	DDR	NA	VCCO_DDR	U15_DQ14
PS_RAM	NA	J20	PS_DDR_A13_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A13
PS_RAM	NA	R20	PS_DDR_A14_502	NA	502	DDR	NA	VCCO_DDR	NC
PS_RAM	NA	H21	PS_DDR_A11_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A11
PS_RAM	NA	P20	PS_DDR_A12_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A12
PS_RAM	NA	U20	PS_DDR_A9_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A9
PS_RAM	NA	M22	PS_DDR_A10_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A10
PS_RAM	NA	J21	PS_DDR_A7_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A7
PS_RAM	NA	T20	PS_DDR_A8_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A8
PS_RAM	NA	N22	PS_DDR_A5_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A5
PS_RAM	NA	L20	PS_DDR_A6_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A6
PS_RAM	NA	L22	PS_DDR_A3_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A3
PS_RAM	NA	M20	PS_DDR_A4_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A4
PS_RAM	NA	W21	PS_DDR_VRP_502	NA	502	DDR	NA	GND	PULL DOWN
PS_RAM	NA	V21	PS_DDR_VRN_502	NA	502	DDR	NA	VCCO_DDR	PULL UP

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
PS_RAM	NA	R21	PS_DDR_CKP_502	NA	502	DDR	NA	VCCO_DDR	U15/16_CKP
PS_RAM	NA	P21	PS_DDR_CKN_502	NA	502	DDR	NA	VCCO_DDR	U15/16_CKN
PS_RAM	NA	N21	PS_DDR_A2_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A2
PS_RAM	NA	K20	PS_DDR_A1_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A1
PS_RAM	NA	K22	PS_DDR_A0_502	NA	502	DDR	NA	VCCO_DDR	U15/16_A0
PS_RAM	NA	R22	PS_DDR_BA2_502	NA	502	DDR	NA	VCCO_DDR	U15/16_BA2
PS_RAM	NA	T22	PS_DDR_BA1_502	NA	502	DDR	NA	VCCO_DDR	U15/16_BA1
PS_RAM	NA	U22	PS_DDR_BA0_502	NA	502	DDR	NA	VCCO_DDR	U15/16_BA0
PS_RAM	NA	Y22	PS_DDR_ODT_502	NA	502	DDR	NA	VCCO_DDR	U15/16_ODT
PS_RAM	NA	Y21	PS_DDR_CS_B_502	NA	502	DDR	NA	VCCO_DDR	U15/16_CS_B
PS_RAM	NA	U21	PS_DDR_CKE_502	NA	502	DDR	NA	VCCO_DDR	U15/16_CKE
PS_RAM	NA	V22	PS_DDR_WE_B_502	NA	502	DDR	NA	VCCO_DDR	U15/16_WE_B
PS_RAM	NA	Y23	PS_DDR_CAS_B_502	NA	502	DDR	NA	VCCO_DDR	U15/16_CAS_B
PS_RAM	NA	V23	PS_DDR_RAS_B_502	NA	502	DDR	NA	VCCO_DDR	U15/16_RAS_B
PS_RAM	NA	R26	PS_DDR_DQ16_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ4
PS_RAM	NA	P24	PS_DDR_DQ17_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ1
PS_RAM	NA	N26	PS_DDR_DQ18_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ2
PS_RAM	NA	P23	PS_DDR_DQ19_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ3
PS_RAM	NA	P26	PS_DDR_DM2_502	NA	502	DDR	NA	VCCO_DDR	U16_LDM
PS_RAM	NA	P25	PS_DDR_DQS_P2_502	NA	502	DDR	NA	VCCO_DDR	U16_LDQS_P
PS_RAM	NA	R25	PS_DDR_DQS_N2_502	NA	502	DDR	NA	VCCO_DDR	U16_LDQS_N
PS_RAM	NA	T24	PS_DDR_DQ20_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ0
PS_RAM	NA	T25	PS_DDR_DQ21_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ5
PS_RAM	NA	T23	PS_DDR_DQ22_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ6
PS_RAM	NA	R23	PS_DDR_DQ23_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ7
PS_RAM	NA	V24	PS_DDR_DQ24_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ12
PS_RAM	NA	U26	PS_DDR_DQ25_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ9
PS_RAM	NA	U24	PS_DDR_DQ26_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ10
PS_RAM	NA	U25	PS_DDR_DQ27_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ11
PS_RAM	NA	V26	PS_DDR_DM3_502	NA	502	DDR	NA	VCCO_DDR	U16_UDM
PS_RAM	NA	W24	PS_DDR_DQS_P3_502	NA	502	DDR	NA	VCCO_DDR	U16_UDQS_P
PS_RAM	NA	W25	PS_DDR_DQS_N3_502	NA	502	DDR	NA	VCCO_DDR	U16_UDQS_N
PS_RAM	NA	W26	PS_DDR_DQ28_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ13
PS_RAM	NA	Y25	PS_DDR_DQ29_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ8
PS_RAM	NA	Y26	PS_DDR_DQ30_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ14
PS_RAM	NA	W23	PS_DDR_DQ31_502	NA	502	DDR	NA	VCCO_DDR	U16_DQ15
MGT_PWR	NA	AA4	MGTAVCC	NA	NA	NA	NA	MGTAVCC	+1V
MGT_PWR	NA	AA8	MGTAVCC	NA	NA	NA	NA	MGTAVCC	+1V
MGT_PWR	NA	AB6	MGTAVCC	NA	NA	NA	NA	MGTAVCC	+1V
MGT_PWR	NA	AC8	MGTAVCC	NA	NA	NA	NA	MGTAVCC	+1V
MGT_PWR	NA	AD6	MGTAVCC	NA	NA	NA	NA	MGTAVCC	+1V

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
MGT_PWR	NA	AE8	MGTAVCC	NA	NA	NA	NA	MGTAVCC	+1V
MGT_PWR	NA	R4	MGTAVCC	NA	NA	NA	NA	MGTAVCC	+1V
MGT_PWR	NA	T6	MGTAVCC	NA	NA	NA	NA	MGTAVCC	+1V
MGT_PWR	NA	U4	MGTAVCC	NA	NA	NA	NA	MGTAVCC	+1V
MGT_PWR	NA	Y6	MGTAVCC	NA	NA	NA	NA	MGTAVCC	+1V
MGT_PWR	NA	AB2	MGTAVTT	NA	NA	NA	NA	MGTAVTT	+1V2
MGT_PWR	NA	AC4	MGTAVTT	NA	NA	NA	NA	MGTAVTT	+1V2
MGT_PWR	NA	AD2	MGTAVTT	NA	NA	NA	NA	MGTAVTT	+1V2
MGT_PWR	NA	AE4	MGTAVTT	NA	NA	NA	NA	MGTAVTT	+1V2
MGT_PWR	NA	AF2	MGTAVTT	NA	NA	NA	NA	MGTAVTT	+1V2
MGT_PWR	NA	AF6	MGTAVTT	NA	NA	NA	NA	MGTAVTT	+1V2
MGT_PWR	NA	T2	MGTAVTT	NA	NA	NA	NA	MGTAVTT	+1V2
MGT_PWR	NA	V2	MGTAVTT	NA	NA	NA	NA	MGTAVTT	+1V2
MGT_PWR	NA	W4	MGTAVTT	NA	NA	NA	NA	MGTAVTT	+1V2
MGT_PWR	NA	Y2	MGTAVTT	NA	NA	NA	NA	MGTAVTT	+1V2
MGT_PWR	NA	V6	MGTVCCAUX	NA	NA	NA	NA	MGTVCCAUX	+1V8
VCCINT	NA	L11	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	L13	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	L15	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	M12	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	N11	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	N15	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	P12	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	R11	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	R15	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	T12	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	T14	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	U11	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	U13	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCINT	NA	U15	VCCINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCAUX	NA	N9	VCCAUX	NA	NA	NA	NA	VCC_AUX_PL_PS	+1V8
VCCAUX	NA	P8	VCCAUX	NA	NA	NA	NA	VCC_AUX_PL_PS	+1V8
VCCAUX	NA	R9	VCCAUX	NA	NA	NA	NA	VCC_AUX_PL_PS	+1V8
VCCAUX	NA	T8	VCCAUX	NA	NA	NA	NA	VCC_AUX_PL_PS	+1V8
VCCAUX	NA	U9	VCCAUX	NA	NA	NA	NA	VCC_AUX_PL_PS	+1V8
VCCAUX	NA	V10	VCCAUX	NA	NA	NA	NA	VCC_AUX_PL_PS	+1V8

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
VCCAUX_IO_G0	NA	M10	VCCAUX_IO_G0	NA	NA	NA	NA	VCC_AUX_IO	+2V0
VCCAUX_IO_G0	NA	P10	VCCAUX_IO_G0	NA	NA	NA	NA	VCC_AUX_IO	+2V0
VCCAUX_IO_G0	NA	T10	VCCAUX_IO_G0	NA	NA	NA	NA	VCC_AUX_IO	+2V0
VCCO_0	NA	V12	VCCO_0	NA	0	NA	NA	VCC_0_MIO0	+3V3
VCCO_0	NA	V14	VCCO_0	NA	0	NA	NA	VCC_0_MIO0	+3V3
VCCO_12	**X1:83**	AA16	VCCO_12	NA	12	HR	X1_2	VIO_X1_2	USER DEF
VCCO_12	**X1:84**	AB13	VCCO_12	NA	12	HR	X1_2	VIO_X1_2	USER DEF
VCCO_12	NA	AC10	VCCO_12	NA	12	HR	NA	VIO_X1_2	USER DEF
VCCO_12	NA	AD17	VCCO_12	NA	12	HR	NA	VIO_X1_2	USER DEF
VCCO_12	NA	AE14	VCCO_12	NA	12	HR	NA	VIO_X1_2	USER DEF
VCCO_12	NA	AF11	VCCO_12	NA	12	HR	NA	VIO_X1_2	USER DEF
VCCO_13	**X1:29**	AA26	VCCO_13	NA	13	HR	X1_1	VIO_X1_1	USER DEF
VCCO_13	**X1:30**	AB23	VCCO_13	NA	13	HR	X1_1	VIO_X1_1	USER DEF
VCCO_13	NA	AC20	VCCO_13	NA	13	HR	NA	VIO_X1_1	USER DEF
VCCO_13	NA	AE24	VCCO_13	NA	13	HR	NA	VIO_X1_1	USER DEF
VCCO_13	NA	AF21	VCCO_13	NA	13	HR	NA	VIO_X1_1	USER DEF
VCCO_13	NA	Y19	VCCO_13	NA	13	HR	NA	VIO_X1_1	USER DEF
VCCO_33	NA	E4	VCCO_33	NA	33	HP	NA	VCCO_DDR	+1V35
VCCO_33	NA	F1	VCCO_33	NA	33	HP	NA	VCCO_DDR	+1V35
VCCO_33	NA	H5	VCCO_33	NA	33	HP	NA	VCCO_DDR	+1V35
VCCO_33	NA	J2	VCCO_33	NA	33	HP	NA	VCCO_DDR	+1V35
VCCO_33	NA	L6	VCCO_33	NA	33	HP	NA	VCCO_DDR	+1V35
VCCO_33	NA	M3	VCCO_33	NA	33	HP	NA	VCCO_DDR	+1V35
VCCO_34	**X2:85**	A6	VCCO_34	NA	34	HP	X2_2	VIO_X2_2	USER DEF
VCCO_34	**X2:86**	B3	VCCO_34	NA	34	HP	X2_2	VIO_X2_2	USER DEF
VCCO_34	NA	C10	VCCO_34	NA	34	HP	NA	VIO_X2_2	USER DEF
VCCO_34	NA	D7	VCCO_34	NA	34	HP	NA	VIO_X2_2	USER DEF
VCCO_34	NA	G8	VCCO_34	NA	34	HP	NA	VIO_X2_2	USER DEF
VCCO_34	NA	K9	VCCO_34	NA	34	HP	NA	VIO_X2_2	USER DEF
VCCO_35	**X2:31**	A16	VCCO_35	NA	35	HP	X2_1	VIO_X2_1	USER DEF
VCCO_35	**X2:32**	B13	VCCO_35	NA	35	HP	X2_1	VIO_X2_1	USER DEF
VCCO_35	NA	E14	VCCO_35	NA	35	HP	NA	VIO_X2_1	USER DEF
VCCO_35	NA	F11	VCCO_35	NA	35	HP	NA	VIO_X2_1	USER DEF
VCCO_35	NA	H15	VCCO_35	NA	35	HP	NA	VIO_X2_1	USER DEF
VCCO_35	NA	J12	VCCO_35	NA	35	HP	NA	VIO_X2_1	USER DEF
VCCBRAM	NA	M16	VCCBRAM	NA	NA	NA	NA	+1V_GLOBAL	+1V
VCCBRAM	NA	P16	VCCBRAM	NA	NA	NA	NA	+1V_GLOBAL	+1V
VCCBRAM	NA	T16	VCCBRAM	NA	NA	NA	NA	+1V_GLOBAL	+1V
VCCBRAM	NA	V16	VCCBRAM	NA	NA	NA	NA	+1V_GLOBAL	+1V
VCCO_DDR	NA	H25	VCCO_DDR_502	NA	502	NA	NA	VCCO_DDR	+1V35
VCCO_DDR	NA	J22	VCCO_DDR_502	NA	502	NA	NA	VCCO_DDR	+1V35

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
VCCO_DDR	NA	L26	VCCO_DDR_502	NA	502	NA	NA	VCCO_DDR	+1V35
VCCO_DDR	NA	M23	VCCO_DDR_502	NA	502	NA	NA	VCCO_DDR	+1V35
VCCO_DDR	NA	N20	VCCO_DDR_502	NA	502	NA	NA	VCCO_DDR	+1V35
VCCO_DDR	NA	R24	VCCO_DDR_502	NA	502	NA	NA	VCCO_DDR	+1V35
VCCO_DDR	NA	T21	VCCO_DDR_502	NA	502	NA	NA	VCCO_DDR	+1V35
VCCO_DDR	NA	V25	VCCO_DDR_502	NA	502	NA	NA	VCCO_DDR	+1V35
VCCO_DDR	NA	W22	VCCO_DDR_502	NA	502	NA	NA	VCCO_DDR	+1V35
VCCPAUX	NA	L19	VCCPAUX	NA	NA	NA	NA	VCC_AUX_PL_PS	+1V8
VCCPAUX	NA	N19	VCCPAUX	NA	NA	NA	NA	VCC_AUX_PL_PS	+1V8
VCCPAUX	NA	R19	VCCPAUX	NA	NA	NA	NA	VCC_AUX_PL_PS	+1V8
VCCPAUX	NA	U19	VCCPAUX	NA	NA	NA	NA	VCC_AUX_PL_PS	+1V8
VCCPINT	NA	L17	VCCPINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCPINT	NA	N17	VCCPINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCPINT	NA	P18	VCCPINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCPINT	NA	R17	VCCPINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCPINT	NA	T18	VCCPINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCPINT	NA	U17	VCCPINT	NA	NA	NA	NA	VCC_INT_PL_PS_BRAM	+1V0
VCCPLL	NA	M18	VCCPLL	NA	NA	NA	NA	VCC_PLL_PS	+1V8
VCCO_MIO0_500	NA	A26	VCCO_MIO0_500	NA	500	NA	NA	VCC_0_MIO0	+3V3
VCCO_MIO0_500	NA	B23	VCCO_MIO0_500	NA	500	NA	NA	VCC_0_MIO0	+3V3
VCCO_MIO0_500	NA	E24	VCCO_MIO0_500	NA	500	NA	NA	VCC_0_MIO0	+3V3
VCCO_MIO1_501	NA	C20	VCCO_MIO1_501	NA	501	NA	NA	VCC_MIO1	USER DEF
VCCO_MIO1_501	NA	D17	VCCO_MIO1_501	NA	501	NA	NA	VCC_MIO1	USER DEF
VCCO_MIO1_501	NA	F21	VCCO_MIO1_501	NA	501	NA	NA	VCC_MIO1	USER DEF
VCCO_MIO1_501	NA	G18	VCCO_MIO1_501	NA	501	NA	NA	VCC_MIO1	USER DEF
VCCO_MIO1_501	NA	K18	VCCO_MIO1_501	NA	501	NA	NA	VCC_MIO1	USER DEF
DDR_VREF	NA	K21	PS_DDR_VREF0_502	NA	502	DDR	NA	+0V75_VREF	+0V625
DDR_VREF	NA	M21	PS_DDR_VREF1_502	NA	502	DDR	NA	+0V75_VREF	+0V625
GND	**X1:27**	NA	GND	NA	NA	NA	X1_1	GND	
GND	**X1:28**	NA	GND	NA	NA	NA	X1_1	GND	
GND	**X1:55**	NA	GND	NA	NA	NA	X1_1	GND	
GND	**X1:56**	NA	GND	NA	NA	NA	X1_1	GND	
GND	**X1:81**	NA	GND	NA	NA	NA	X1_2	GND	
GND	**X1:82**	NA	GND	NA	NA	NA	X1_2	GND	
GND	**X1:109**	NA	GND	NA	NA	NA	X1_2	GND	MGT
GND	**X1:110**	NA	GND	NA	NA	NA	X1_2	GND	MGT

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
GND	**X1:115**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:116**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:121**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:122**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:127**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:128**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:133**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:134**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:139**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:140**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:145**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:146**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:151**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:152**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:157**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:158**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:163**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X1:164**	NA	GND	NA	NA	NA	X1_MGT	GND	MGT
GND	**X2:5**	NA	GND	NA	NA	NA	X2_1	GND	
GND	**X2:6**	NA	GND	NA	NA	NA	X2_1	GND	
GND	**X2:33**	NA	GND	NA	NA	NA	X2_1	GND	
GND	**X2:34**	NA	GND	NA	NA	NA	X2_1	GND	
GND	**X2:59**	NA	GND	NA	NA	NA	X2_2	GND	
GND	**X2:60**	NA	GND	NA	NA	NA	X2_2	GND	
GND	**X2:87**	NA	GND	NA	NA	NA	X2_2	GND	
GND	**X2:88**	NA	GND	NA	NA	NA	X2_2	GND	
GND	**X2:113**	NA	GND	NA	NA	NA	X2_CFG	GND	
GND	**X2:114**	NA	GND	NA	NA	NA	X2_CFG	GND	
GND	**X2:125**	NA	HW_RESET_IN	NA	NA	NA	NA	NA	
GND	**X2:126**	V15	V_BATT_IN	NA	NA	NA	NA	NA	2.0V max
GND	**X2:137**	NA	GND	NA	NA	NA	X2_MIO	GND	MIO
GND	**X2:138**	NA	GND	NA	NA	NA	X2_MIO	GND	MIO
GND	**X2:153**	NA	GND	NA	NA	NA	X2_MIO	GND	MIO
GND	**X2:154**	NA	GND	NA	NA	NA	X2_MIO	GND	MIO
POWER_IN	**X2:1**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X2:2**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X2:3**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X2:4**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X2:165**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X2:166**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X2:167**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3

Module Function	Module Pin	FPGA Pin	Pin Name	Byte Group	Bank	I/O Type	I/O Group	I/O Voltage source	Remark
POWER_IN	**X2:168**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:1**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:2**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:165**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:166**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:167**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3
POWER_IN	**X1:168**	NA	3V3_in	NA	NA	NA		+3V3_GLOBAL	+3V3

Compliance

All KRM modules are ROHSII and REACH compliant. For further details, customers may request the current declaration of conformity by emailing office@knowres.ch.
All KRM Modules are manufactured with UL94V-0 flammability rated PCBs with an IPC Class2 quality rating.

Electrical Specification

ESD

KRM Modules are sensitive to electrostatic discharge and must be handled with proper ESD precautions.

Absolute Maximum Ratings[i]

Symbol	Description	Min	Max
POWER_IN	Global power in	-0V5	3V6
VCCO_12/13	HR Bank I/O power supply	-0V5	3V6
VCCO_34/35	HP Bank I/O power supply	-0V5	2V0
V_BATT_IN	Encryption key storage supply	-0V5	2V0
PS_IO	MIO Bank I/O signal levels	-0V5	2V0
PL_IO_HP	HP Bank I/O signal levels	-0V5	2V0
PL_IO_HR	HR Bank I/O signal levels	-0V5	3V6

Recommended Operating conditions

Symbol	Description	Min	Typ	Max
POWER_IN	Global power in	3V2	3V3	3V4
VCCO_12/13	HR Bank I/O power supply	3V2	3V3	3V4
VCCO_34/35	HP Bank I/O power supply	1V7	1V8	1V89
V_BATT_IN	Encryption key storage supply	1V0	--	1V89
PS_IO	MIO Bank I/O signal levels[ii]	-0V2	--	VCCO + 0V2
PL_IO_HP	HP Bank I/O signal levels	-0V2	--	VCCO + 0V2
PL_IO_HR	HR Bank I/O signal levels	-0V2	--	VCCO + 0V2

[i] Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied.
Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect module reliability

[ii] For I/O operation, refer to the Xilinx *7 Series FPGAs SelectIO Resources User Guide* (UG471) or the Xilinx *Zynq-7000 SoC Technical Reference Manual* (UG585).

Thermal specification

Absolute Maximum Ratings[iii]

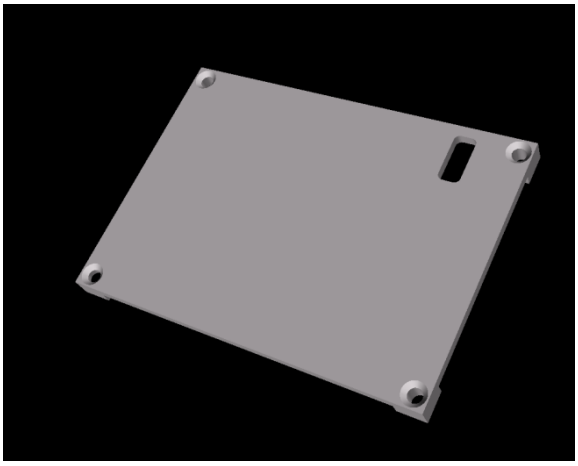
Symbol	Description	Min	Max
Delta T	Max temperature change per second while operating	--	+/-1°C/sec
TSTG	Storage temperature ambient un-powered	-40°C	+125°C

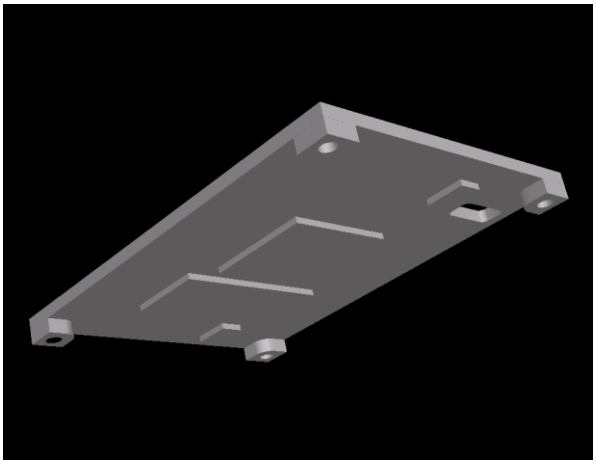
Recommended Operating Conditions

Symbol	Description	Min	Typ	Max
Tj C	Operating Junction temperature of FPGA for commercial grade	0°C	--	+70°C
Tj I	Operating Junction temperature of FPGA for industrial grade	-40°C	--	+85°C
Delta T	Allowed temperature change per second while operating	--	--	+/-0.5°C/sec

Heat Management

The thermal load of the Module depends greatly on the user application, and is driven by clock speed, toggle rate, logic utilization, active peripherals and CPU utilization. The user must ensure that the generated heat is adequately removed from the module so that the Recommended Operating Conditions are not exceeded.
In order to ensure a consistent thermal interface across all KRM-3xxx module variants, KR offers a module-specific heat-spreader plate. The plate is simply an adapter and is not designed as a standalone cooling solution. In some low power applications of the smaller module variants, the spreader plate may be sufficient as a standalone solution.





[iii] Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the module. These are stress ratings only, and functional operation of the module at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied.

Module configurations

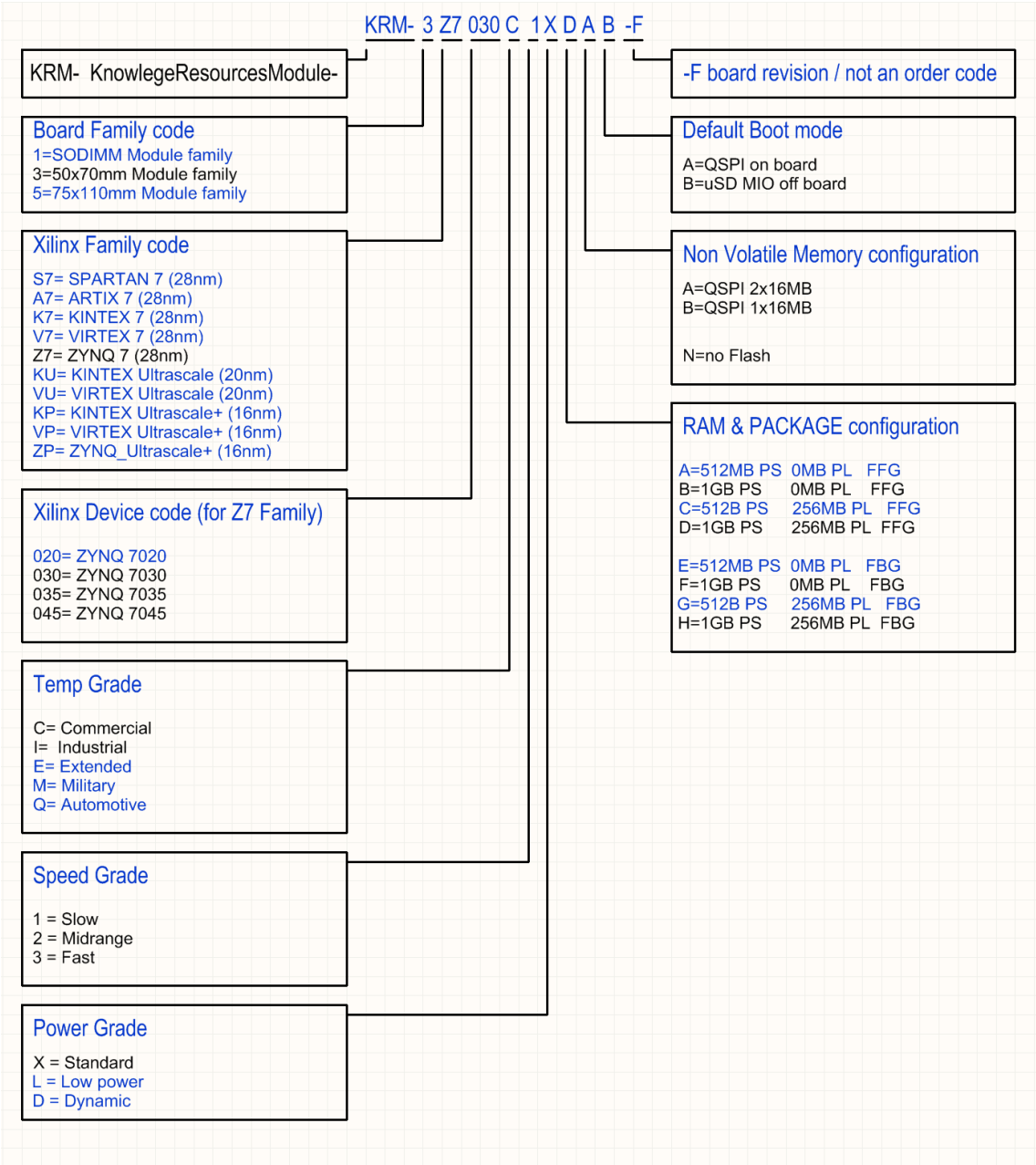
The KRM3-Z7xxx Modules can be purchased in a multitude of configurations as shown in the table below. Option codes shown in black are valid options for this family, not all valid options may be combined (for example boot option set to on-board QSPI, but no Flash populated is invalid)
Blue option codes may become future options of this module family.

Standard Low quantity configuration

The standard assembly variant, which is orderable as samples, is as follows:

KRM-3Z7030C1XDAB-F or KRM-3Z7030C1XHAB-F

50x70mm module family, with a Zynq 7030, commercial speed grade, standard power rating, 1GB PS RAM and 256MB PL RAM, dual QSPI (32MB total) populated and boot mode set to external SD card interface with FFG or FBG SoC package.
Configuration table



Module Identification

Xilinx is no longer labeling its parts with speed grade and temperature grade information. The KRM PCB is also only labelled with the generic family code (KRM-3Z7030-45) and contains no clear text information about its configuration. This makes it all but impossible to identify the modules detailed configuration.

All modules as of Board Rev_E can be identified by scanning the QR code label that is mounted on the PS DDR memory components. The QR code contains a unique URL that will query the database of the KR test system and will produce a PDF document that contains information about the factory configuration of the module and test sequence the module passed after production.

Errata

- POK and CFG done LED labels swapped on REV A PCB
  - The outermost LED is labelled CFG, it reports POK from the onboard regulators
  - The second LED is labelled POK, it reports successful configuration of the SoC

  This is corrected on all later revisions of the PCB